Anritsu Advancing beyond

White paper

PCIe® 6.0: Testing for a New Generation

Overview

PCI-SIG® is developing PCI Express® (PCIe) 6.0 to meet the high-speed data transmission needs of emerging applications. With the doubling of data rates and other enhanced performance specifications, PCIe 6.0 will add complexity to high-speed interconnect designs. Engineers need to select the proper signal integrity test solutions to verify that their products are compliant with the new PCIe 6.0 standards.

This paper outlines the enhanced PCIe 6.0 technologies, such as PAM4, Forward Error Correction (FEC) and link equalization. It also provides guidelines on selecting the proper test system to verify PCIe 6.0 designs.

PCIe 6.0 is Fast Approaching

PCI-SIG is fast at work in developing the next generation of PCIe interconnect I/O technology for high-speed devices, including hard drives, solid state drives (SSDs), graphics cards, Wi-Fi routers, and internal Ethernet connections. PCIe 6.0, currently at Rev 0.5 of the specification with Rev 0.7 in progress, is slated for finalization in 2021. That timeline means signal integrity engineers need to already begin integrating PCIe 6.0 into their design plans.

PCIe Specification	Data Rate (GT/s) (Encoding)	x16 B/W per dirn**	Year
1.0	2.5 (8b/10b)	32 GT/s	2003
2.0	5.0 (8b/10b)	64 GT/s	2007
3.0	8.0 (128b/130b)	126 GT/s	2010
4.0	16.0 (128b/130b)	252 GT/s	2017
5.0	32.0 (128b/130b)	504 GT/s	2019
6.0 (WIP)	64.0 (PAM-4, Flit)	1024 GT/s (~1 Tb/s)	2021*

Table 1: *PCIe data rates by generation.*

Table 1 shows the data rates of each generation. When jumping from 32 GT/s associated with PCIe 5.0 to 64 GT/s for PCIe 6.0, the PSI-SIG standards committee only slightly altered the compliance requirements. To address signal degradation, tighter channel and connector loss and reflections parameters have been implemented. Minor improvements in receiver and transmitter equalization have been made, as well. No major innovations to address the expected complications associated with the steeper rise-fall times, narrower unit intervals (UIs), and greater insertion loss associated with doubling the data rates have been instituted.

For signal integrity engineers, verifying PCIe 6.0 designs will require high-level test solutions that can accurately measure performance to ensure compliance. While many of the tests are similar to those of previous generations, the complexity of PCIe 6.0 tests and accuracy necessary require test instruments that have distinct performance thresholds.

* Projected

** Bandwidth after encoding overhead

PCIe 6.0 Leverages PAM4

One change in PCIe 6.0 is 32 Gbaud PAM4 signaling. The previous five generations of the specifications all leverage NRZ. PAM4 will allow the specification's channel reach to remain similar to that of the PCIe 5.0 specification. Like all previous PCIe generations, PCIe 6.0 will be fully backwards compatible, so NRZ will also be supported.

Even though the underlying frequency is the same as the PCIe 5.0 specification at 32.0 GT/s NRZ, there will be extra circuitry and logic involved for the PAM4 mode to track three eyes, along with the logic changes needed to operate in Flow Control Unit (FLIT) mode. FLIT was selected for PCIe 6.0 architecture because it allows error correction to operate on fixed-sized packets. Since error correction happens on FLIT, the Cyclic Redundancy Check (CRC) and retry must be done at the FLIT level. Once the link operates in FLIT mode, any speed change to lower data rates will also have to use the same FLIT mode.

In addition to PAM4, the PCIe 6.0 specification includes error assumptions, including correlation between errors on a lane, as well as across lanes. PCIe 6.0 technology uses a unique approach to maintain low latency through a combination of relatively lower First Bit Error Rate (FBER) combined with a light-weight, low latency Forward Error Correction (FEC) for initial correction. A robust CRC then detects any errors that remain after correction. The result is a link level retry, which is also very low latency.

Unlike networking standards that have 100+ nsec of FEC latency, PCIe technology is a load-store protocol. Therefore, it must strictly maintain all specifications, especially in terms of latency, power and high bandwidth. Using FEC and CRC will allow PCIe 6.0 to achieve the specified low latency with latency reduction in most cases. It will also achieve low complexity and a low bandwidth overhead.

Performance to Meet Emerging Applications

PCI-SIG is establishing performance for the new generation of high-speed interconnects to meet emerging applications, such as IoT, automotive, and AI. Table 2 shows the key specifications of PCIe 6.0. The same infrastructure as the PCIe 5.0 specification for lane margining in terms of voltage and time margining are being used in the PCIe 6.0 specification.

Metrics	Requirements
Data Rate	64 GT/s, PAM4 (double the bandwidth per pin every generation)
Latency	<10 ns adder for Transmitter + Receiver over 32.0 GT/s (including FEC)
Bandwidth Inefficiency	<2 % adder over PCIe 5.0 across all payload sizes
Reliability	0 < FIT << 1 for a x16 (FIT – Failure in Time, number of failures in 109 hours)
Channel Reach	Similar to PCIe 5.0 specification under similar set up for Retimer(s) (maximum 2)
Power Efficiency	Better than PCIe 5.0 specification
Low Power	Similar entry / exit latency for L1 low-power state Addition of a new power state (L0p) to support scalable power consumption with bandwidth usage without interrupting traffic

Table 2: *Summary of PCIe 4 and 5 standards.*

The evolution to PAM4 technology, as well as other enhanced specifications under the 6.0 standards development will affect testing of I/O interfaces and systems utilizing PCIe 6.0. Many of the tests – including Bit Error Rate (BER), link equalization, and FEC – are already being conducted to verify designs with existing PCIe technologies. The parameters of those measurements for PCIe 6.0, however, are much more complex due to the new standards.

PAM4 Effect on BER

PAM4 signaling alleviates channel loss because it runs at half the frequency with two bits per UI. Because PCIe 6.0 has three eyes in the same UI, however, there will be reduced eye height and width. As a result, the BER will be several levels of magnitude higher with PAM4, which is why FEC is necessary.

For PCIe 6.0, BER is a combination of the FBER, correlation of errors in a lane, and correlation of errors across lanes. FBER is the probability of the first bit error occurring at a receiver in a link. PSI-SIG conducted extensive studies before finalizing the 10^{-6} FBER for PCIe 6.0. It is a critical number to satisfy the <10 ns latency requirement. It also reduces the bandwidth overhead so it is <2% impact, which is another requirement.

There are two primary mechanisms to correct the errors in a lane and those across lanes. The most notable are through FEC and detection of errors by CRC, resulting in the eventual correction through link layer retry. FEC operates on the principle of sending redundant data that can be deployed to correct some errors at the receiver. CRC is an error detection code used to authenticate packet transmission between the sender and the receiving end.

Importance of FEC

PCI-SIG has established a low latency FEC of <2 ns for PCIe 6.0 and that is to be part of the specified overall signal latency of <10 ns. FEC is based on a fixed number of symbols. Because of this, it is simple to transition to FLITs, as they are fixed size, as well. Link frequency is 64 GT/s.

The FEC logic can be run at any frequency. In general, the expectation is that the logic will operate at 1G (or 500 MHz or 2G) and easily reach a latency far exceeding 2 ns. PCI-SIG recommends a lightweight FEC for correction. The very robust CRC for detection, combined with a fast link level replay, handles any errors that the FEC cannot correct. As long as the replay probability of a FLIT is approximately 10^{-6}, there is no appreciable performance impact either due to the FEC latency or the replay latency in case of an undetected error. A combination of FEC correction and CRC detection results in a replay that effectively corrects nearly all common errors.

A recommended approach is to establish a FEC symbol error threshold. By doing so, engineers have broader control over error conditions that affect patterns during capture by ignoring insignificant events that are normally corrected in the FEC environment.

To set a threshold, a BERT generates a PAM4 signal to the Device Under Test (DUT) receiver input. The DUT determines the logic state of the input signal and loop decision to transmitter output for the error signal in the BERT for analysis. The BERT's built-in Error Detector (ED) determines if the DUT's decision was correct. For relevant results, the BERT's jitter and noise profiles must be standards-compliant.

When conducting the test, it's important to note that a random error is not nearly as meaningful as one that occurs in a burst. FEC generally cannot be corrected beyond a certain limit. Post processing must be done beyond that limit to help determine why the DUT might be misreading an incoming symbol. With this approach, engineers have the ability to test a device using standard PRBS patterns while basing error detection capture on events that might be problematic in an FEC environment.

Link Equalization

Link training and stressed receiver tolerance are simultaneously evaluated using a stressed signal in the link equalization test. Two tests – for receivers and transmitters – must be performed using SigTest software developed by the PCI-SIG.

Figure 1 shows a diagram of CEM or BASE testing. In a CEM test, the DUT consists of both the SerDes and the add-in card to which it is mounted. In a BASE test, the DUT consists of the SerDes itself and is mounted to a system board.

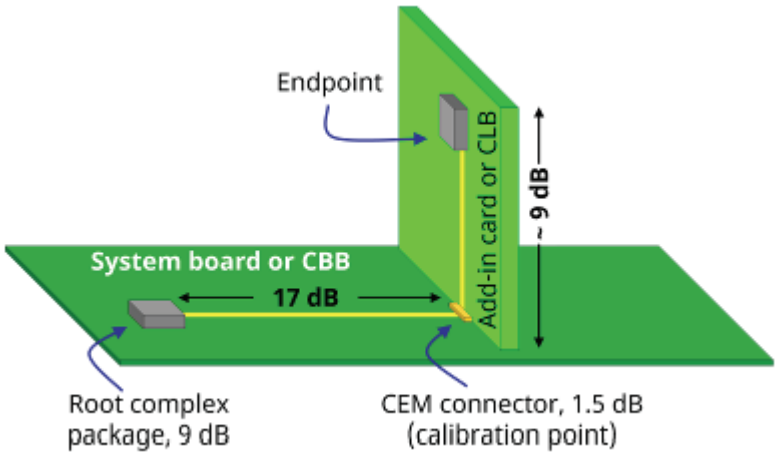

Figure 1: *Diagram of a CEM or BASE testing configuration.*

Receiver Link Equalization – Similar to a standard stressed eye receiver BER, receiver link equalization has one notable difference. The DUT must first perform link negotiation to correctly compensate for the test channel. The idea of stressed receiver tolerance testing is to submit the DUT-receiver to the worst-case signal that still complies with the specification.

Prior to the test being conducted, the signal being transmitted from the BERT must be precisely calibrated to mimic the worst-case signal at the end of the test channel. The test signal has jitter and interference impairments that include random jitter (RJ), sinusoidal jitter (SJ), sinusoidal differential mode interference (DMI), and common mode interference (CMI), as shown in figure 2.

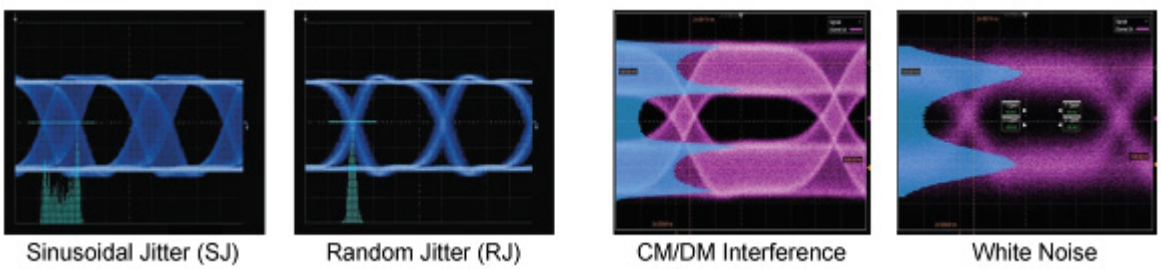

Figure 2: *Screenshots of signal impairments applied by the Anritsu MP1900A PPGs.*

After calibrating the transmitter emphasis and jitter settings, the test process requires multiple iterations of SigTest software to determine the proper test channel and impairment mix. A "variable ISI" test board with several differential trace lengths with losses ranging from 34 dB to 37 dB in 0.5 dB steps is used to apply different amounts of loss and ISI. The DUT-add-in card (DUT-AIC) must be capable of training the link with this maximally stressed signal. Once the link is trained and the transmitter FFE and receiver equalization schemes are optimized, the DUT-receiver must operate at BER $<10^{-6}$.

Figure 3 shows the test setup. The BERT PPG differential output is split so that the signal is transmitted to both the DUT-receiver and the oscilloscope. The DUT-transmitter output is also divided so its signal is transmitted to the oscilloscope and the BERT ED, which acts as reference receiver.

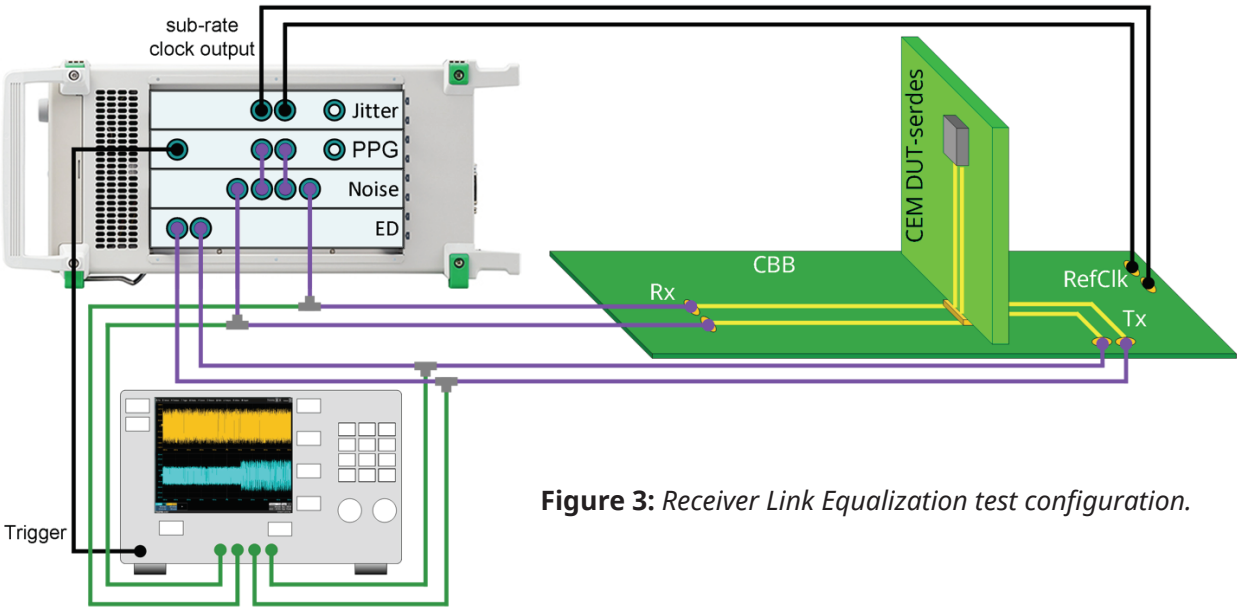

Figure 3: *Receiver Link Equalization test configuration.*

The test begins with the BERT PPG transmitting a preset request to the DUT-transmitter—a negotiation in the PHY layer logical sub-block. The DUT responds by changing its FFE taps. The oscilloscope also receives the preset request. It must have a level of protocol functionality to identify the preset request to measure (tReq). The trigger signal of the oscilloscope is an option to tReq but it adds uncertainty to the measurement due to the time-delay of the trigger cable.

Transmitter Link Equalization – This is a required compliance test that verifies that the device correctly changes equalization within the specified time when requested by the link partner. The BERT requests an equalization change from the devices that simultaneously sends a trigger to the oscilloscope so the time delay to the DUT can be measured in the electrical domain.

The BERT PPG sends requests to the DUT-transmitter through the PCIe physical layer logic-sub-block protocol (Figure 4). The BERT PPG sequentially sends requests to the DUT-AIC for every FFE preset at each PCIe data rate. The DUT-transmitter modifies its FFE scheme and transmits the signals. The DUT-transmitter output is split so that its signal is sent to both the oscilloscope and the BERT ED. The oscilloscope observes the high-level equalization change required while the ED serves as a reference receiver that confirms the preset change.

The BERT uses the PPG auxiliary output to trigger the oscilloscope acquisition of each signal. The oscilloscope captures the waveforms with every FFE preset and every data rate. It then runs SigTest installed on the oscilloscope to evaluate each waveform according to the compliance requirements. Reports on the results can also be created through SigTest.

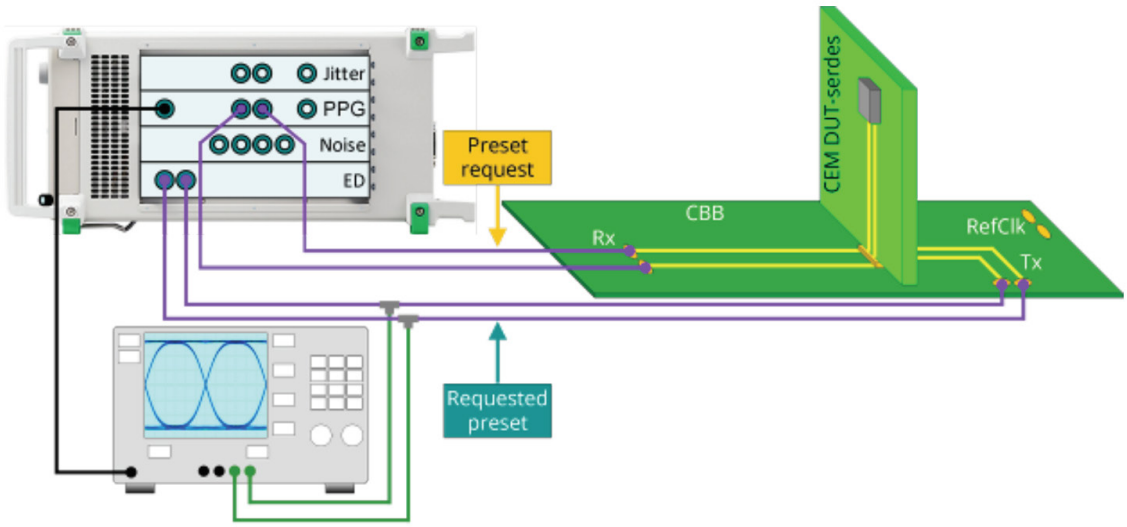

Figure 4: *Transmitter Link Equalization test setup.*

Benefits of JTOL

The jitter tolerance test (JTOL) is not required by the PCIe 6.0 specification, but it is an excellent method to determine if a receiver can tolerate different amplitudes and frequencies of jitter. Similar to link equalization tests, a stressed signal based on the worst case that still falls within compliance is used. It has ISI, RJ, DMI and CMI. As a debug technique or performance margin analysis, JTOL can be tested with any equalization scheme. SJ is then added to the signal, according to the amplitude-frequency template shown in Figure 5.

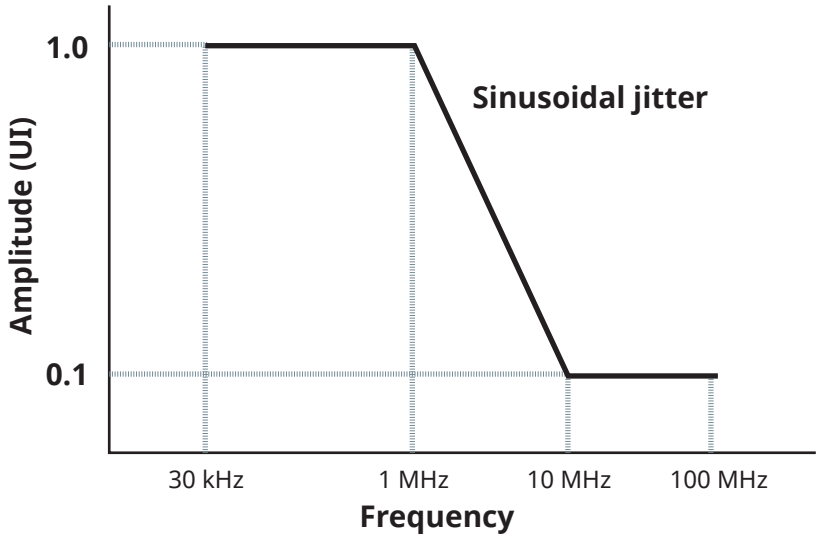

Figure 5: *Amplitude-frequency template to determine JTOL.*

High amplitude jitter is applied at low frequencies and low amplitude jitter is applied at high frequencies. The rolloff, from 1 MHz to 10 MHz, follows the specified CDR frequency response. BER is measured across the template. DUT-receivers should adhere to BER $<10^{-6}$ for all amplitude-frequency pairs. To make the measurement in a reasonable length of time, BER is usually measured to BER $<10^{-3}$ and the slope of the BER probability is extrapolated to assure BER $<10^{-6}$.

Selecting the Proper Test System

To conduct these tests accurately, PCIe 6.0 test systems need a feature-rich, protocol-aware bit error rate tester (BERT) and an oscilloscope. The BERT needs a built-in instrument-quality PPG that can apply precise levels of specific signal impairments and a built-in ED capable of verifying compliance with the PCIe specifications. The BERT should have multiple NRZ pattern-generating channels and error detectors that operate at 32 GT/s and PAM4 channels at 64 GT/s to support PCIe 6.0 and earlier generations.

Low intrinsic jitter of 115 fs and 12 ps 20 to 80% rise/fall times are also required for signal integrity. The BERT needs to apply every required signal impairment in amplitude ranges that exceed those required by the PCIe 6.0 specifications, as outlined in Table 3.

RJ with amplitude from 0 to 0.5 UIpp covering 10 kHz to 1 GHz bandwidth
SJ at amplitudes from 0 to 2000 UI; modulation frequencies from 10-100 kHz; 0 to 1 UI from 10 MHz to 250 MHz
Second SJ tone at 33 kHz, 87 MHz, 100 MHz and 210 MHz
Spread-spectrum clocking (SSC) at modulation frequencies from 28 kHz to 37 kHz; amplitudes from 0 to 7000 ppm
Sinusoidal DMI from 2 to 10 GHz
Sinusoidal CMI from 0.1 to 6 GHz

Table 3: *Key specifications of BERT for PCIe 6.0.*

The oscilloscope should have real-time sampling bandwidth > 50 GHz. For both transmitter signal evaluation and calibration of stressed-eye receiver tolerance tests, the oscilloscope must also support PCI-SIG test software analysis tools. In particular, it should have:

> Automated link equalization testing	> Eye diagram and jitter analysis
> Automated test fixture de-embedding	> PCIe PHY logical sub-block protocol decoding

Conclusion

The evolution of PCIe to 6.0 is creating new design challenges for signal integrity engineers. Sound testing processes utilizing a system comprised of a protocol-aware BERT and high-speed oscilloscope that produce high-quality eye diagrams and have comprehensive analysis tools will create greater confidence in complex high-speed designs for emerging applications, especially data center products and systems.

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Specifications are subject to change without notice.

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