

# Improved SAR ADCs Further Expand Design Options

**Sponsored by Texas Instruments: Myriad mid-range industrial applications can take advantage of the technological strides made with SAR ADCs, such as the inclusion of decimation filters.**

**P**ractically every electronic design attempted today involves an analog-to-digital converter (ADC). In simple applications, the ADC inside an accompanying MCU may be adequate, while extreme-high-frequency applications require high-speed ADCs. Other designs require special attention to the type and characteristics of the data converter.

Design challenges such as the analog input filter usually need extra time. Don't forget features like decimation, which offers benefits in some designs. The suggestions presented in this article may help with these various design considerations.

## ADC Selection

Three basic types of ADCs are commonly used today: delta-sigma, successive-approximation register (SAR), and gigasample-per-second (GSPS) flash or pipelined ADCs for RF use. Your application will dictate the types of signals that must be digitized. These are the main specifications to match up to your design needs:

- **Sampling rate:** The basic rule is to sample at a rate that must be two or more times greater than the highest-frequency content of the signal to be digitized. Stated another way, a frequency of half the sampling rate is called the Nyquist frequency; it's the highest-frequency signal that can be converted without aliasing. If this criterion isn't met, aliasing will occur. Aliasing creates new signals that interfere with the conversion.
- **Resolution:** This specification defines the precision of the conversion. Resolution is stated in terms of the smallest increment of input voltage that can be measured. Resolution is set by the number of bits in the output. The greater the number of bits, the higher the resolution.

- **Dynamic range:** This is the maximum range of input voltage levels between highest and lowest expressed in dB. Related to this spec is the spurious-free dynamic range (SFDR) that defines the range between the highest input amplitude and the peak spur in the noise floor.
- **Latency:** The time between the initiation of the sampling pulse and the appearance of the output bits.
- Other factors that affect ADC selection are the *noise floor* and the *signal-to-noise ratio (SNR)*.
- Power consumption may be a major concern in your application. Power usage usually scales with sampling rate.

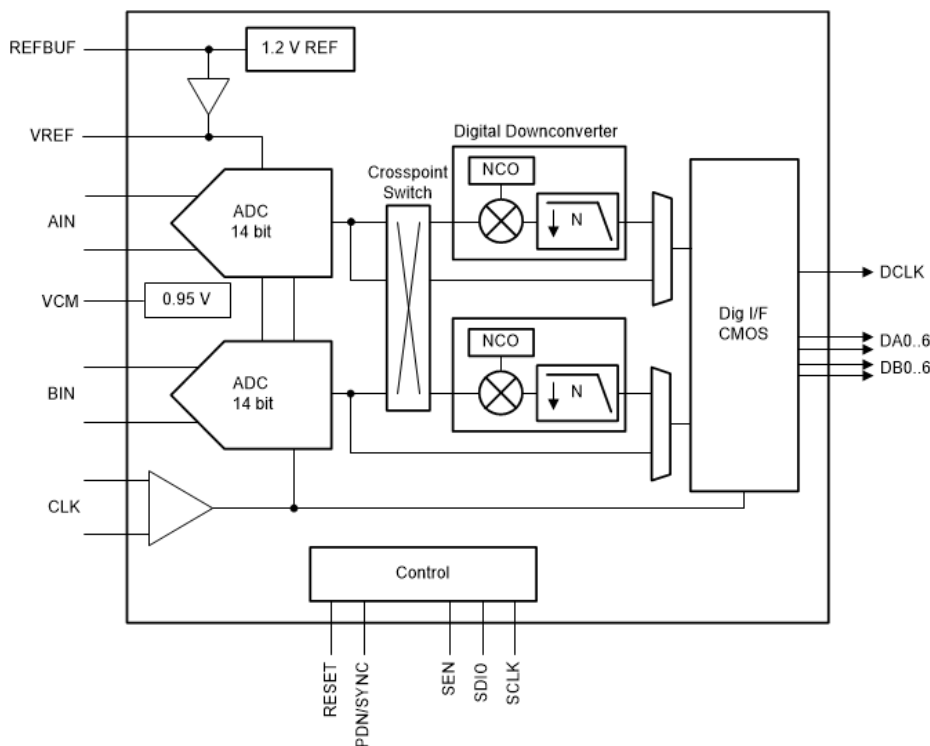
The first two factors are usually identified at the outset; then an ADC architecture is selected. Delta-sigma ADCs deliver the most resolution with digital outputs of up to 32 bits. However, sampling rates are commonly below 10 megasamples per second (MSPS).

[SAR converters offer resolutions up to 18 bits and sampling rates up to 125 MSPS.](#) This mid-range category fits many applications. GSPS ADCs, which can provide sampling rates of over 10 GSPS and resolutions to 10 to 14 bits, are found mainly in RF equipment and products like cell phones.

For a wide range of general applications, such as industrial equipment, the SAR is a good choice. The delta-sigma ADC is a solid option when there's a need for high precision.

## Essential Design Criteria

All ADCs require an analog input filter. Its main purpose is to restrict the input bandwidth to only the signal to be digitized. Other signals, especially higher-frequency components at the input, can produce aliasing that creates conversion errors. This requires a low-pass filter with sharp roll



Shown is a block diagram of TI's ADC364x SAR DAC.

off for frequencies above the highest-frequency component in the desired signal.

Analog low-pass filters are effective, but they can be large and complex to deal with when trying to achieve the desired attenuation. Digital filters like the finite-input-response (FIR) filter with an adequate number of taps can provide superior selectivity.

Perhaps the easiest way to minimize input filter requirements is to use a sampling rate considerably higher than the minimum needed for aliasing protection. Such oversampling increases the distance between the input signal and the aliasing signals, thereby relaxing the input filter requirements.

Keep in mind that a higher sampling rate may be too fast for the MCU, FPGA, or other circuits receiving the ADC output. [A decimation filter can be used after the conversion to lower the output rate.](#) Decimation offers the additional advantage of reducing the anti-aliasing filter requirements because the low-pass filter effects of the decimation circuit will lower second- and third-order harmonics. Decimation also improves the SNR by  $-3$  dBFS (decibels full scale) for each factor of 2.

The most critical part of any design using an ADC is the analog front end (AFE). In addition to the aliasing filter, most ADCs require some impedance-matching circuits, bias networks, and connections to the ADC reference volt-

age. All of these must be customized to your application. External components are usually necessary, therefore plan for some additional PCB space in your design.

### An ADC to Consider

Texas Instruments offers a line of SAR ADCs that can match up with many applications. One example is the [ADC364x, a dual-channel 14-bit CMOS device that can sample at rates from 10 to 65 MSPS](#) (see figure). Inputs can be single-ended or differential. Outputs may be parallel or serial using standard CMOS or LVDS outputs. External resistors on the output control the current.

A key feature is its on-chip digital filter with decimation. Decimation effectively reduces the output data rate so

that slower external devices like an MCU or FPGA may be accommodated. Decimation by 2, 4, 8, 16, or 32 may be selected.

Designing with ADCs is a sophisticated process with many interrelated factors to be considered. Time spent searching for the best available ADC will pay off later in design time and cost savings.