

## Using PoL DC-DCs to Solve Voltage Accuracy, Efficiency, and Latency Issues

Rather than implement a space-consuming controller FET solution to handle high currents, a monolithic PoL converter with internal FETs might be the right answer for your design.

roximity to power. It's one of the best ways to improve voltage accuracy, efficiency, and the dynamic response of a power rail. A point-ofload (PoL) converter is a power-supply dc-dc converter placed as close to the load as possible to achieve proximity to power.

Applications that benefit from PoL converters include highperformance CPUs, SoCs, and FPGAs-all

ION  $4.91 \,\mathrm{m}\Omega \times 10 \,\mathrm{A} = 49.1 \,\mathrm{m}\mathrm{V}$ VIN Length: 50 mm Width: 5 mm RUN/SS TG Thickness: 35 µm SW CPU (10 A Load) BOOST 1.00 V 0.951 V SGND INTV<sub>CC</sub> No Margin BG PGOOD PGND  $V_{FB}$ 

1. Shown is dc-dc output voltage drop with narrower PCB trace.

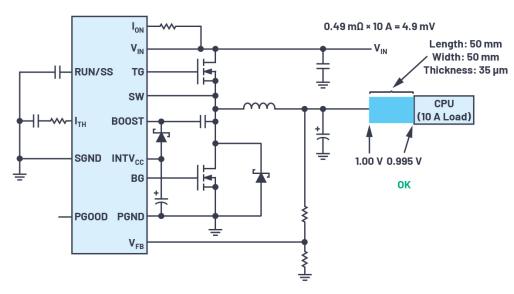
of which require ever-increasing power levels. In automotive applications, for example, the number of sensors used for an advanced driver-assistance system (ADAS)—such as those in radar, LiDAR, and vision systems—is steadily multiplying. Thus, faster data processing (more power) is needed to detect and track surrounding objects with minimal latency.

Many of these digital systems operate at high currents and low voltages, increasing the need to minimize the distance from power supply to load. One obvious problem with high currents is trace-induced voltage drops from converter to load. Figures 1 and 2 show how minimizing the resistance of the leads between supply and load minimizes the output voltage drop of the converter's output-in this case, a controller IC and MOSFETs powering a CPU.

The wider PCB trace shown in Figure 2 reduces the voltage drop to meet the accuracy requirement, but parasitic inductance must also be considered. The PCB trace length in Figure 2 has an estimated inductance of about 14.1 nH, as shown in the LTspice model of *Figure 3*.

Because inductance suppresses dynamic changes in current (di/dt) when loads change, the current passing through this parasitic inductance is limited by its time constant, deteriorating transient response. What results from parasitic inductance are voltage droops, as shown in the simulation plot in Figure 4.

Placing a converter near the load minimizes the effect of PCB resistance and parasitic inductance. The dc-dc converter IC should be placed at the nearest possible location to the CPU. Note that Figures 1 and 2 show the schematic for a traditional high-current power supply—namely, switch-mode controller and external FETs. Controller FET solutions can handle the high-current loads required by the applications mentioned above. The problem with a controller solution is the external FETs have space requirements that can make it difficult to produce a true PoL regulator solution (Fig. 5).

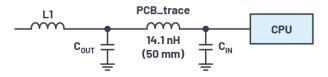


2. Here, dc-dc output voltage drop occurs with a wider PCB trace.

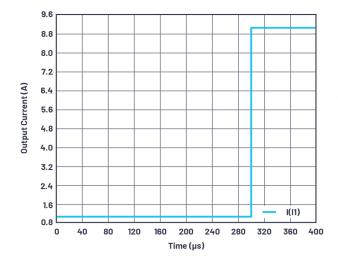
One alternative to a controller is a monolithic solution where the FETs are internal to the converter IC. For instance, the LTC3310S monolithic step-down regulator (3-  $\times$ 3-mm IC footprint) enables point-of-load solutions up to 10 A for one IC, and 20 A with parallel multiple ICs. These ICs are shown in Figures 6 and 12, respectively. The tiny footprint makes possible PoL placement (Fig. 7).

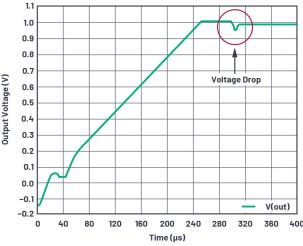
In addition to its small package size, the LTC3310S supports a maximum switching frequency of 5 MHz-high-frequency operation reduces the necessary output capacitance and overall solution PCB footprint. Figure 8 shows the load transient performance of LTC3310S, where an 8-A load change results in an output-voltage excursion of less than ±40 mV, achieved with only 110-μF output capacitance.

Despite the obvious advantages of using high-powered monolithic PoL converters, there's a possible deal breaker: heat. If the converter produces too much heat, it won't survive when used in an already hot system.

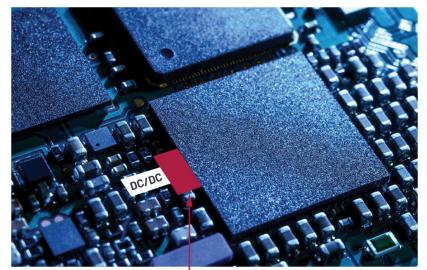


3. An LTspice model for the PCB trace inductance.

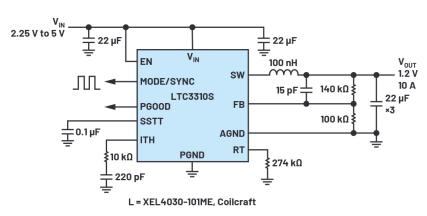




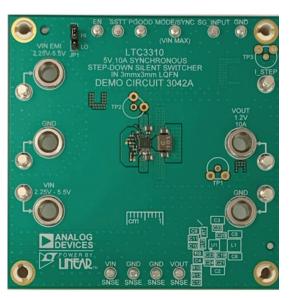
4. A dc-dc output voltage dip with a transient current.



Short and Wide PCB Trace



6. Shown is an LTC3310S step-down regulator.



7. The tiny LTC3310S footprint enables PoL placement.

## 5. Ideal placement of a dc-dc converter to the CPU.

In the solution proposed above, the LTC3310S internal temperature rise is minimized through high efficiency operation, enabling it to reliably run even in the severe temperature conditions surrounding power-hungry components such as CPUs, SoCs, and FPGAs (Fig. 9). Furthermore, the LTC3310S includes accurate internal temperature sensors, which allows for the measurement of the internal junction temperature through the SSTT pin (Fig. 10), with the resulting temperature sensor characteristic shown in Figure 11.

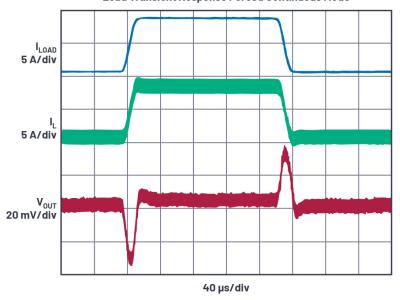
Certain monolithic regulators can be scaled to higher load applications through multiphase, parallel operation. Figure 12 shows multiple LTC3310S devices connected in parallel and operated out of phase to double the current capability.

The controller's clock is set by a single resistor on the RT pin, with the relative phase(s) of subnode(s) programmed through a resistor divider on the RT pin. In the case shown in Figure 12, RT is grounded to set the subnode to 180 degrees phase-shifted from the controller.

Figure 13 shows the inductor current and output ripple current for a twochannel converter, as depicted in Figure 12. In-phase performance is compared with dual, antiphase performance. Antiphase operation reduces output ripple current (via cancellation) from 14 A p-p (single-phase) to 6 A p-p (dual-phase) without additional external filters.

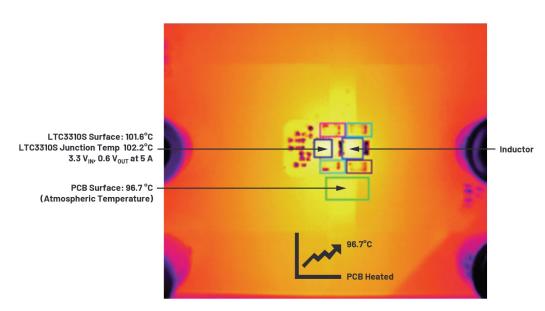
Atsuhiko Furukawa joined Linear Technology (now part of Analog Devices) in 2006. He has provided technical support for various applications to small and mid-size customers for over 10 years. He transitioned to the automotive segment in 2017 and is now designing huge (several kilowatts) as well as small safety automotive applications. Atsuhiko is a marathon runner with his best record of 3 hours and 3 minutes.

## Load Transient Response Forced Continuous Mode

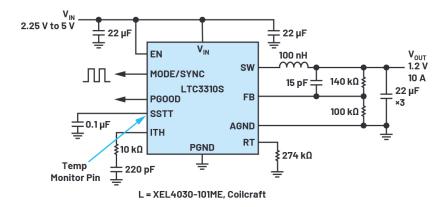


3.3  $V_{IN}$  to 1.2  $V_{OUT}$ , 2 MHz  $C_{OUT}$  = 110  $\mu$ F, L = 100 nH Load Step: 1 A to 9 A 1 A/µs Slew Rate

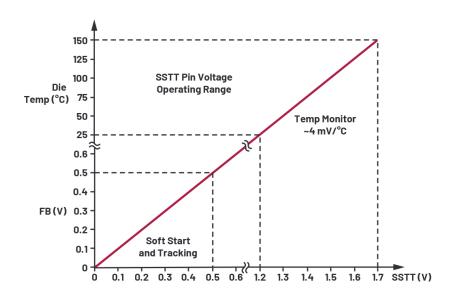
8. The transient response of the LTC3310S.



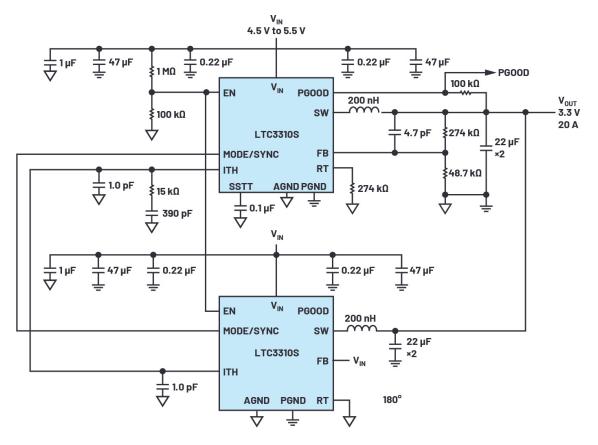
9. A thermal camera image of the LTC3310S.



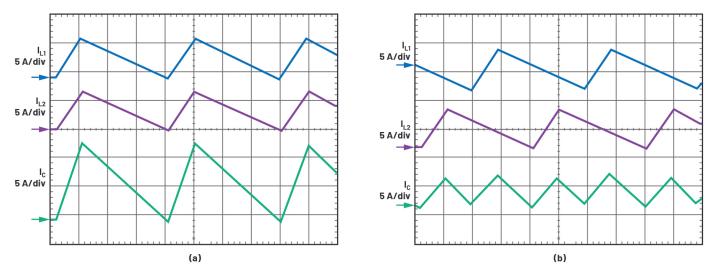
10. An LTC3310S temperature sense pin.



11. Soft-start and temperature-monitoring operation.



12. A 20-A, dual-phase monolithic regulator POL solution.



13. Comparing the inductor current and output current in two versions of a two-channel converter: channels in-phase (a) vs. antiphase (b).