MENTOR TARGETS HIERARCHICAL DFT AND AUTOMOTIVE SAFETY

By **Rick Nelson,** Interim Chief Editor

Hierarchical DFT methodology and automotive functional safety have been two recent areas of focus for Mentor, a Siemens business. Legacy design-for-test flows impose inefficiencies when transitioning to a hierarchical methodology, according to Geir Eide, product marketing director, Tessent Design-for-Test, at Mentor. What's required for fast time to market, he said in a recent phone interview, is optimal end-to-end automation for hierarchical implementation. And with respect to automotive functional safety, the required tools and technologies extend beyond DFT to embrace a safety ecosystem that included third-party tools, added Eide's colleague Lee Harrison, automotive IC test solutions manager at Mentor.

To address both automation for hierarchical implementation and automotive functional safety, Mentor in November introduced two new solutions. First, the Tessent Connect DFT automation methodology delivers intent-driven hierarchical test implementation that helps IC design teams achieve manufacturing test quality goals faster and with fewer resources compared with traditional DFT methods. Second, Mentor also introduced the Tessent Safety ecosystem, which leverages the automotive IP portfolio of Arm as part of a Functional Safety Partnership Program.

Hierarchical DFT

Eide explained that advanced IC designs can achieve high defect coverage for manufacturing and in-system test by making use of dedicated on-chip infrastructure such as embedded compression, built-in self-test, and IEEE 1687 Tessent Connect IJTAG networks. But as IC designs grow in size and integrate more on-chip IP, engineers are increasingly adopting hierarchical DFT approaches that break down the traditional DFT process into smaller, more manageable elements.

DFT is becoming a critical path to tape-out, said Eide, adding, "The transition to hierarchical DFT methodologies is inevitable." Without automation, he explained, engineers need to describe what they want the tools to do each step of the way, information from one step must be carried over to the next, and errors discovered late in the process can result in time-consuming iterations. With intent-driven automation, engineers can use fewer, shorter scripts, with the tool handling integration, setup, and pattern generation, resulting in shorter turnaround time and reliable, sustainable flows.

"Tessent Connect is the optimal way of implementing the Tessent Shell Flow for Hierarchical Designs," Eide noted.

Eide said an early adopter of Tessent Connect is eSilicon, a provider of FinFET ASICs, market-specific IP platforms, and advanced 2.5D packaging solutions. By employing Tessent Connect, he said, eSilicon improved IC DFT implementation cost while enabling system-level DFT testing and debug capabilities for a sophisticated next-generation ASIC.

"eSilicon uses Tessent Connect to help us meet our aggressive production schedules and deliver industry-leading ICs like those based on eSilicon's neuASIC 7-nm platform for machine learning," said Joseph Reynick, director of DFT services at eSilicon, in a press release. "As design complexity continues to grow, our system/OEM customers' needs expand from just focusing on high-quality IC manufacturing test to also providing effective in-system test and functional debug capabilities. With today's complex 2.5D/3D devices, we are not shipping in volume until our chips are fully operational in our customers' systems, including DFT and IP test. It would be very difficult to meet these challenges without the Tessent DFT portfolio and the efficiencies gained from Tessent Connect automation."

As part of the Tessent Connect rollout, Mentor also announced the Tessent Connect Quickstart program,
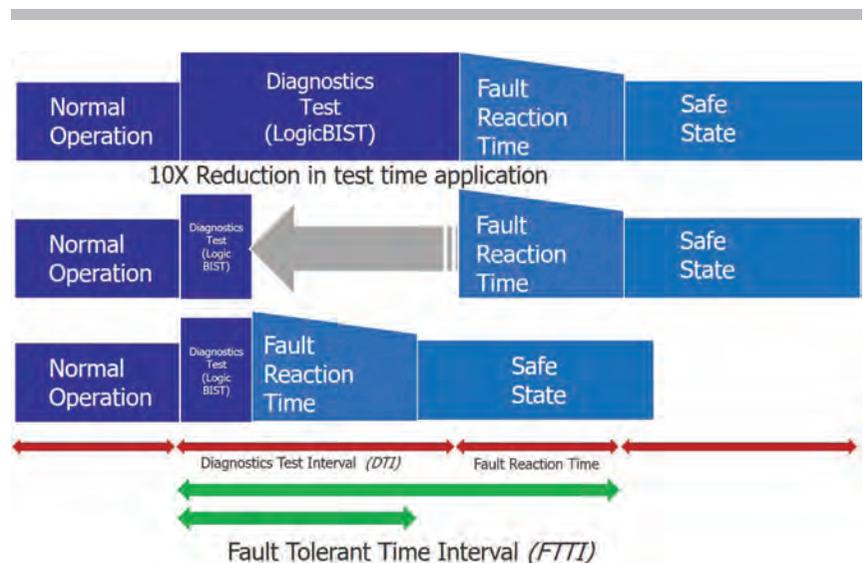
▲ **Figure 1:** FTTI reduction enabled by Tessent LogicBIST with Observation Scan technology.

offering detailed flow assessments and customized insights from Mentor's applications and consulting services engineers to help IC design teams optimize and automate their DFT processes when using Tessent Connect.

"The Tessent Connect Quickstart program is the fastest way to elevate your DFT flow to Tessent Connect," concluded Eide.

Automotive functional safety

Mentor describes its new Tessent Safety Ecosystem as a portfolio of its automotive IC test solutions with links to its partners, providing an alternative to competing programs based on closed, monolithic, single-source models.

"New requirements require new test techniques or safety mechanisms, outside of the scope of traditional DFT," explained Harrison. "Monitoring and managing all of the different in-system test functions is now critical to the safe operation of an automotive IC. This often requires a dedicated safety island or manager." He added that in-system logic test time, with a defined fault-tolerant time interval (FTTI), is now a critical component of meeting safety requirements (**Figure 1**).

"To address the challenge of in-system logic test time," Harrison said, "Tessent LogicBIST with Observation Scan technology (LBIST-OST) can reduce the in-system runtime by 10x, enabling a much reduced FTTI when used in an automotive application."

The Tessent Safety Ecosystem includes the following technologies in addition to the new Tessent LBIST-OST:

- Tessent MemoryBIST, which features an automation flow that provides design rule checking, test planning, integration, and verification at either the RTL or gate level. Because Tessent MemoryBIST features a hierarchical architecture, BIST and self-repair capabilities can be added to individual cores as well as at the top level.
- The Tessent MissionMode product, which provides a combination of automation and on-chip IP for enabling semiconductor chips throughout an automotive electronics system to be tested and diagnosed at any point during a vehicle's functional operation.
- The Tessent DefectSim transistor-level defect simulator for analog, mixed-signal (AMS) and non-scan digital circuits. Suitable for both high-volume and high-reliability ICs, Tessent DefectSim measures defect coverage and tolerance.
- Mentor's participation in the Arm Functional Safety Partnership Program (AFSPP). The Mentor Tessent Safety ecosystem leverages Arm Safety Ready IP functionalities like the Cortex-R52 processor, which combines real-time execution with the integrated functional safety capabilities of any Arm processor, hypervisor technology to simplify software integration, and separation functionality to protect safety-critical code.
- Mentor's automotive-grade automatic test pattern generation (ATPG) technology, which detects defects at the transistor and interconnect levels often missed by traditional test patterns and fault models.
- Close links to Mentor's Austemper SafetyScope and KaleidoScope products, which add safety analysis, autocorrection, and fault-simulation technology to address random hardware faults. Austemper technology analyzes a designer's RTL for faults and vulnerabilities and is capable of smart fault injection to help safety mechanisms react in a planned manner for covered faults. Through parallelized and distributed operation methods, proprietary acceleration algorithms achieve speed-ups of many orders of magnitude over standard gate-level fault injection techniques.

Among the early adopters of key technologies in Mentor's Tessent Safety ecosystem is Renesas, which evaluated Mentor's new Tessent LBIST-OST solution in designing one of its newest automotive processors.

"Leveraging the Observation Scan technology featured in the new Tessent LBIST-OST solution, we were able to reduce the test time for in-system Logic BIST by 5x, thereby enabling a much faster coverage ramp up," said Hideyuki Okabe, director, Digital Design Technology Department, Shared R&D EDA Division, IoT and Infrastructure Business Unit at Renesas Electronics Corp., in a press release. "This enabled us to reduce our Fault Tolerant Time Interval...when using Logic BIST as a safety mechanism and improve the safety response when detecting new defects in our automotive products. We hope to continue to adopt this technology going forward for our automotive products." **EE**