SPECIAL REPORT

SEMICONDUCTOR TEST: VENDORS CHALLENGED BY COST OF TEST AMID INCREASING DEVICE COMPLEXITY

By Mike Hockett, Editor-in-Chief

As the complexity of newer electronics devices increases, so do the demands on providers of semiconductor test. Vendors of test solutions are tasked with not hampering the productivity of designers and always increasing the quality of their test programs—all while keeping the cost of test as low as possible. Such vendors have become used to the innovation demands that come with mobile electronics, but newer avenues like the Cloud, artificial intelligence, and the onset of 5G will provide plenty of obstacles to overcome for years ahead.

To stay abreast of the latest trend developments in semiconductor test, challenges and demands in this area, and what new solutions are on the market, we at *Evaluation Engineering* asked a pool of semiconductor test vendors and partners for their input on these talking points. Read on to see what they told us.

Marvin Test Solutions' GENASYS Semi TS-960 Series.

Advantest's T2000 GPWGD module.

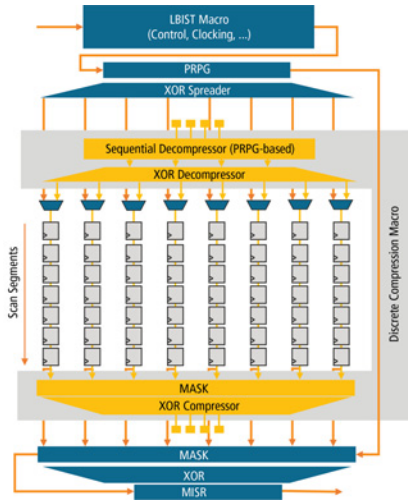
What's trending?

What new or ongoing trends are vendors seeing in the area of semiconductor test?

Rob Knoth, product management director, Digital Staff Group at Cadence Design Systems: "We're seeing an increasing role of test in the functional mission of semiconductors, for example, with memory and logic built-in-self-test (BIST) for in-system test and also with register-transfer level (RTL) insertion of design-for-test (DFT) to help with functional verification and safety. Additionally, it's becoming much more Important for DFT insertion to be tightly integrated with synthesis/place and route, otherwise you are sacrificing too much design power, performance and area, or automatic test pattern generation (ATPG) quality of results (QoR)—test coverage, test time/cost—with an RTL-only approach."

Judy Davies, vice president of global marketing communications at Advantest: "The most significant change to come along in decades is the imminent deployment of 5G technology, which will see widespread use in not only next-generation smart phones, but also the Internet of Things (IoT) and artificial intelligence (AI). With the advent of 5G and 5G-NR communication ICs, test equipment is being asked to support advanced devices that operate at mmWave frequencies to achieve faster transmission speeds, higher bandwidths, higher density connections, and ultra-low latency."

Sausan Arebi, technical writer and Brandon Malatest, chief operating officer at Per Vices: "There has been a large shift toward testing using ATE. This equipment plays a vital role in maintaining the quality and integrity of semiconductor components, as well as handling their new and upcoming transformations and the associated growing complexity of silicon chips.



▲ A diagram showing how Cadence Design System's new Modus DFT Software solution includes two test modes with discrete scan compression and LBIST.

Semiconductor tests require automation and systematic decision-making to better address the ongoing challenges within the testing market. This is coupled with a need for flexible platforms that can handle mixed domain (RF and digital) for the ever-changing needs of the ATE. There has been a recent transition in RF test instrumentation from analog to digital signal processing, as well as more FPGA-based DSP for advanced RF test equipment. Combining these two, new semiconductor test equipment has enabled automated tests, a reduced time to market, and has lowered the overall cost of test. With future ATE systems requiring interoperability, a reduced logistics footprint, and overall improved testing—all while reducing repair time and the rigidity of the system. There is still ongoing improvement possible, making flexibility and adaptability necessary for the success of this technology."

Markus Loerner, market segment manager—industry, components, research & universities at Rohde & Schwarz: "Obviously, speed improvement is an ongoing task. Especially as RF components get more and more complex, more test ports and more frequency coverage like in a handset RFIC supporting more bands and modes (3G, 4G, 5G). Complexity is going up per device. However, the market is expecting reduced cost."

Bob Stasonis, technical product specialist at Pickering Interfaces: "Not necessarily a new issue, but the cost of test is always a hot topic. As the market pushes manufacturers to drive down costs, test is always a culprit. As to newer trends, higher I/O density, lower voltages for isolation testing—with denser chips, the smaller gaps on the die require lower voltages for isolation testing, testing thousands of pins on a single chip, and higher frequencies for microwave devices—5G to 65 GHz is the obvious issue. This may seem a little trite, but in one instance, I asked the test manager what his biggest test problem was, and he replied "Concrete!" Basically, if the tester was too big, as many of the more expensive testers are, the more floor space he needed. So, too much floor space for test systems and he will need to expand his operation—not desirable if you are trying to cut costs. So, the move to smaller, lower-cost modular platforms such as PXI are on the cards."

Jon Semancik, director of marketing at Marvin Test Solutions: "There has been an increase in customer development of application-specific test solutions with a focus on the cost of the tester and reducing the overall cost of test. This is especially true in the emerging areas, such as RF test requirements for 5G and automotive radar, as multiple suppliers strive to be first to market."

Peter Griffiths, director of business development Tektronix: "1: We continue to see a trend into the high-power arena. Demand for more efficient high-voltage semiconductors in 5G, automotive, and alternative energy markets is driving increasingly complex testing and research into new technologies like SiC and GaN. 2: People need to get more done with less equipment and in less time. IOT is one of the drivers here. Providing more capability into a single box and making it quick and easy-to-use drives continual innovation."

Geir Eide, product marketing director—Tessent ATPG & Compression products at Mentor Graphics: "1: Almost 100 companies are racing to dominate the AI chip market. Whoever gets there first wins. This means that the top priority is to get chip samples to the market faster. For test, this translates to getting design-for-test (DFT) out of the critical path, and streamlining silicon bring-up. 2: There are a lot of new entrants to the automotive sector. This means that a lot of design organizations have to ramp up fast on functional safety. This means not just stricter manufacturing test requirements, but a need to translate the traditional test metrics to functional safety metrics. It's not just about detecting defects, it's about detecting the safety-critical defects and ensuring safe operation of the device in the field."

Challenges

What key challenges are vendors or their partners facing in semiconductor test?

Knoth, Cadence: "The challenges that vendors are facing in semiconductor test are that DFT skills are more in demand on all sides—EDA, semiconductor design, architecture, etc. It requires people to solve challenges, and we are all in need of good candidates. Secondly, there are challenges with balancing the cost of test with defective parts per million (DPPM) reduction, and lastly, addressing the smart integration of machine learning in test software is becoming more of a priority."

Davies, Advantest: "To meet the testing requirements of 5G devices, ATE providers must develop reliable, fully integrated, multi-site mmWave test solutions. As one of the first companies to address this emerging market need, Advantest introduced the new V93000 Wave Scale Millimeter system on May 7."

Arebi and Malatest, Per Vices: "Wireless component manufacturers are under pressure to reduce costs, address new technologies, and increase manufacturing flexibility to meet the ever-changing needs of the industry. This is necessary in semiconductor testing, where the products and protocols are evolving and new technology is still not defined. With scalable test architectures, vendors are able to create unique, modular equipment, and reduce the cost of testing. Manufacturers are also finding that vendors' demands are changing where one-off systems are

no longer working for them and there is a demand for adaptable test equipment, offering ease-of-use, durability, and the capability to work on various systems."

Loerner, Rohde & Schwarz: "It is important to work closely with customers to understand the test needs in order to optimize the test solution and work out together the best and most efficient test plan."

Stasonis, Pickering: "Increasing the speed of test often requires parallel testing to improve throughput. There appears to be little new hardware on the test floors we have seen, so test systems are getting old, as chip manufacturers are trying to get by on existing technology. Having said that, we are seeing more do-it-yourself tests systems being built in-house."

Semancik, Marvin Test Solutions: "Vendors face pressures to control costs and improve time to market, which has sparked a move to retrofit existing production test systems with RF test capabilities, providing flexibility to leverage existing test assets where appropriate."

Eide, Mentor: "It's not just about cost and quality anymore; it's about efficient implementation and functional safety. This is new to many IC manufacturers, but also IC vendors."

What are customers asking for?

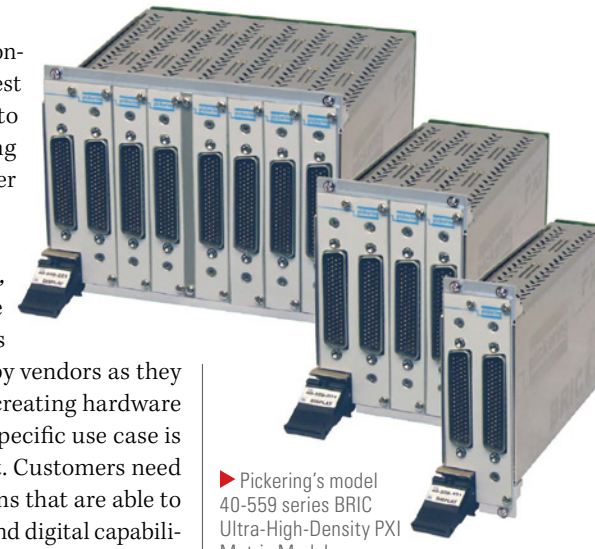
Here are the features and other innovations today's semiconductor test customers are asking vendors to provide.

Knoth, Cadence: "Customers are looking for more of a "left shift" with DFT, making test a job responsibility of the RTL designers as well as implementation, so there's not just the one "test expert." Customers are also looking at balancing the cost of test with DPPM reduction for higher levels of compression, physical awareness, etc. Additionally, they are looking for high ATPG coverage without local power/IR issues."

Davies, Advantest: "One of the few things that remain steadfast in the test market is that integrated device manufacturers and outsourced semiconductor assembly and test companies continue to require greater testing functionality at a lower cost of test."

Arebi and Malatest, Per Vices: "Many of the demands of customers are being addressed by vendors as they are recognizing that creating hardware that matches a very specific use case is becoming insufficient. Customers need customizable platforms that are able to incorporate both RF and digital capabilities in semiconductor test. This demand has been addressed with software defined radios (SDR), which offer a high number of radio channels, high bandwidth and wide operating frequency, and on-board FPGA resources; these attributes are key metrics that enable the necessary inherent flexibility that is being demanded. This flexibility provides additional benefits to customers, allowing test providers to do various tests on one device due to their ability to be programmed to implement any standard, while allowing them to accelerate the process of deploying semiconductor components.

Loerner, Rohde & Schwarz: "The earlier components are tested, the lower value is bound per device and a selection can be done early in the process in order to minimize additional costs on faulty parts by further process steps. Extensive on-wafer test enables an early selection but requires fast and easy adoption and handling of calibrations to get reliable and repeatable results in a challenging environment. We see today not only basic power consumption and test points to be checked, but full RF test from CW to modulated tests already on wafer level."



▶ Pickering's model 40-559 series BRIC Ultra-High-Density PXI Matrix Modules.

Stasonis, Pickering: "The size of tester is brought up. Basically, Semi manufacturers want smaller, lower cost, higher performance. Talk about a challenge!"

Semancik, Marvin Test Solutions: "The move to 5G devices is driving the need for higher frequency RF test capabilities; demands for parallel 40 GHz to 80 GHz test are becoming more commonplace."

Eide, Mentor: "Companies are asking for the ability of test applications to handle larger and more complex semiconductor devices. Those companies are preparing for test earlier in the design flow to be able to reduce the number of iterations and impact of test challenges. A lot of companies are asking for methods to make analog test more efficient."

▶ Per Vices' latest software-defined-radio, Cyan.

Now on the market

Here's what semiconductor test solution vendors told us they've recently made available and what their key features are.

Knoth, Cadence: "The Cadence Modus DFT Software Solution enables designers to reduce SoC design time by up to 3X. It incorporates a patented 2D elastic compression architecture, offering compression ratios beyond 400X without impacting design size or routing. With a complete suite of industry-standard capabilities for memory BIST, logic BIST, test point insertion, and diagnostics, the solution can help designers reduce production test costs and increase silicon profit margins. The Modus 2D elastic compression is an exclusive-or compression logic that forms a physically aware 2D grid across the design floorplan, enabling higher compression ratios with reduced wirelength. The software's unified compression provides an elegant combination of scan compression and logic BIST, with the same physical awareness of 2D Elastic.

Davies, Advantest: "Advantest is constantly developing and introducing new solutions for the global test market. Just this May, we announced a new software enhancement, a module that extends the capabilities of our well-established T2000 tester, and a new test solution for 5G devices: The new V93000 SmartShell software bridge directly links Advantest testers with EDA environments, such as Mentor's Tessent Silicon Insight, to shorten cycle times and get new IC designs to market faster. Our new T2000 GPWGD module (general-purpose waveform generator digitizer) enables testing of high-resolution audio digital-to-analog converters (DACs) embedded in power-management ICs (PMICs) for next-generation audio applications. The V93000 Wave Scale Millimeter system is designed for highly parallel, multisite testing of 5G and 5G-NR mmWave devices and also has the extendibility to handle future needs such as beamforming and over-the-air testing

In addition, our recent acquisition of Astronics' system-level-test products further broadens our solutions portfolio."

▲ Rohde & Schwarz' multiport VNA R&S ZNBT.

Arebi and Malatest, Per Vices: "Our newest release is Cyan, our latest SDR. This multifunctional platform is ideal for RF, as well as test and measurement systems. Addressing many of the challenges facing semiconductor test today, Cyan offers users with a flexible, multichannel solution, that features a customizable number of transmit or receive channels (up to 16 total radio channels) that can be used in testing equipment for a variety of applications and in order to perform multiple duties simultaneously. Cyan aids in accelerating the development and performance necessary to meet new requirements while reducing time-to-market."

Loerner, Rohde & Schwarz: "A vector network analyzer can perform many RF semiconductor tests. Rohde & Schwarz just extended its multiport VNA R&S ZNBT to 40 GHz to address the evolving needs for 5G RF components. The multiport architecture allows parallel test on up to 24 ports. Test on multiport devices, like phased array beamformers or parallel test, support fastest characterization of production lots."

Stasonis, Pickering: "We have focused our efforts on defining a "switching ecosystem", with software products like Switch Path Manager (SPM) automatic signal routing, test sequencing with hardware triggering to improve throughput, developing higher isolation matrices for chip and wafer testing, and working directly with semiconductor manufacturers to give them what they need. High pin-count/isolation reed-relay matrices with multiple analog buses and triggering/test sequencing to support fast parallel testing, plus higher frequency microwave switching are our recent contributions to the industry."

Semancik, Marvin Test Solutions: "MTS' GENASYS Semi (TS-900/960 Series) takes full advantage of the PXI architecture to achieve a cost-effective, full-featured test solution for device, SoC, and SiP test applications, as well as supporting emerging technology development and test. GENASYS Semi provides unique parallel test capabilities, greatly reducing test times for 5G, while minimizing capital equipment expenditures and maximizing the utilization of current test assets."

▼ Keysight's PD1500A power device analyzer with double-pulse tester.

Keysight Technologies: "On May 7, Keysight announced a new dynamic power device analyzer with double-pulse tester, PD1500A, to deliver reliable, repeatable measurements of wide-bandgap semiconductors, while ensuring the safety of the measurement hardware and the professionals performing the tests. Keysight's PD1500A is designed to be modular, allowing many device types to be tested and different characterization tests to be performed at a variety of power levels. The initial system provides complete double-pulse test characterization and parameter extraction for Si and SiC power semiconductors with ratings up to 1.2 kV and 200 A. Additional modules will be added to the PD1500A in the future to perform tests on devices requiring more current, such as GaN and power modules."

◀ Tektronix' S535 Multi-Site Test System.

Griffiths, Tektronix: "1: A new product for this year is the S535 Multi-Site Test System. Targeted at functional or acceptance testing, it is a high-power, high-speed, fully automated solution for testing analog, wide bandgap, mixed-signal, and discrete devices in applications across the semiconductor fab workflow. By testing multiple devices on multiple sites at the same time, the S535 can more-than-double a semiconductor fab's wafer test capacity and significantly lower their cost of ownership profile. 2: This year, we are augmenting our Graphical Touchscreen Source Measurement (SMU) line with a new high voltage/lower current source measure unit, the 2470, to extend the characterization of high voltage, low leakage semiconductors."

Eide, Mentor: "Mentor recently introduced automotive-grade automatic test pattern generation (ATPG) technology for the Tessent TestKompress product. This ensures efficient testing and test metrics for the hardest-to-detect defects for manufacturing test. Mentor has also introduced ATE-Connect to the Tessent SiliconInsight product in collaboration with ATE vendors Teradyne and Advantest. ATE-Connect dramatically simplifies the silicon bring-up process, by allowing DFT and test engineers to interactively communicate directly with test instruments embedded on-chip."

Cohu: Cohu's new HSI2x instrument for the well-established Diamondx ATE platform is optimized for testing clock-embedded and clock-forwarded serial interfaces commonly found in mobile, consumer, industrial, and automotive electronics. These ports connect modems, cameras, displays, storage, and applications processors to enable high bandwidth, low power consumption, and low EMI. The HSI2x instrument features 32 transmit lanes and 24 receive lanes with up to 12.8 Gbps data rate. The instrument can be used for test of high-speed serial ports, such as HDMI, MIPI, JESD204, PCI Express, SATA, EDP, Vby1, and USB3." EE