

# Implementing a Frequency Multiplier Using Mixed-Signal nmable Devices

Here's a concrete design solution on how to implement a frequency multiplier using mixed-signal programmable GreenPAK devices.

his article describes how to implement a frequency multiplier using a GreenPAK programmable mixed-signal IC. The frequency multiplier can be used in a range of applications, including control circuits and communication devices.

#### **Terms and Definitions**

- Define acronyms and abbreviations used in the document. Use camel case for acronym definitions.
- CD: Counter data
- CNT: Counter
- DCMP: Digital comparator
- FSM: Finite state machine

See the *table* on next page for the pin configuration.

The complete design file is available at this link. This circuit design was created in free GUI-based GreenPAK Designer software, a part of the Go Configure Software Hub package.

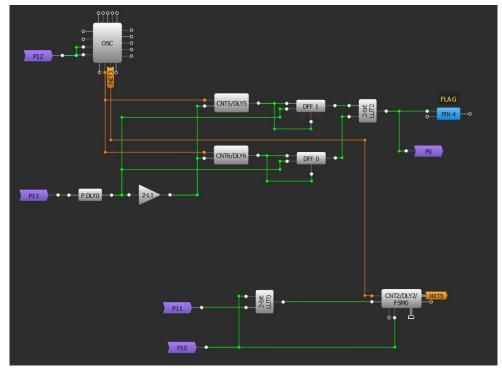
### **Design Overview**

The overall GreenPAK design is shown in Figures 1 and

The design can be divided into the following blocks:

- Frequency multiplier
- Selector
- Multiplier settings
- FLAG
- OUT

Frequency Multiplier



1. GreenPAK Design FLAG Circuit

# **Pin Configuration**

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Pin #	Pin name	Туре	Pin description	Internal resistor
1	VDD	PWR	Supply Voltage	
2	NC		Keep Floating or Connect to GND	
3	NC		Keep Floating or Connect to GND	
4	FLAG	Digital Output	Push Pull 1X	floating
5	NC		Keep Floating or Connect to GND	
6	NC		Keep Floating or Connect to GND	
7	NC		Keep Floating or Connect to GND	
8	NC		Keep Floating or Connect to GND	
9	NC		Keep Floating or Connect to GND	
10	NC		Keep Floating or Connect to GND	
11	GND	GND	Ground	
12	IN	Digital Input	Digital Input without Schmitt trigger	1MΩ pulldown
13	NC		Keep Floating or Connect to GND	
14	NC		Keep Floating or Connect to GND	
15	NC		Keep Floating or Connect to GND	
16	OUT	Digital Output	Push Pull 1X	floating
17	NC		Keep Floating or Connect to GND	
18	NC		Keep Floating or Connect to GND	
19	NC		Keep Floating or Connect to GND	
20	NC		Keep Floating or Connect to GND	

The design includes two frequencymultiplier blocks consisting of FSM0/ DCMP0 and FSM1/ DCMP2, as shown in Figure 3.

The frequency-multiplier block that consists of FSM1/DCMP2 operates as follows: When the signal from the selector is LOW, then FSM1 counts the IN frequency, and when the signal from the selector is HIGH, then FSM1, CNT8, and DCMP2 generate an OUT frequen-

Selector

The selector chooses which of the two blocks counts input frequency and which generates the multiplied output frequency (Fig. 4).

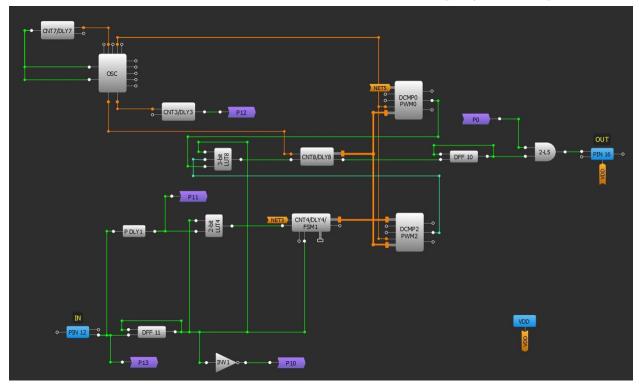
Multiplier Settings

CNT3 is used to select a factor by which the input frequency is multiplied (Fig. 5). The counter data is determined by the formula:

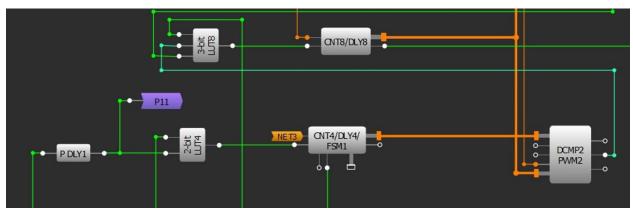
$$CD = 2 * N - 1$$

where CD is counter data and N is the multiplying factor.

CNT7 is used to determine the input frequency. The counter period should be



2. GreenPAK Design Out Circuit (continued)



3. Frequency multiplier

approximately:

 $T \approx 1/(100 \cdot F \cdot N)$ 

where T is the counter period, F is the approximate input frequency, and N is the multiplying factor.

FLAG

For a given input frequency the circuit multiplexer range is between 0.2x and 5x. If the frequency is outside of this range, then FLAG will be LOW (Fig. 6).

OUT

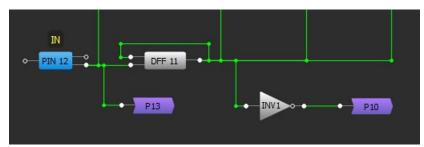
If FLAG is HIGH, DFF10 generates the output frequency with a 50% duty cycle. If FLAG is LOW, then OUT will be LOW (Fig. 7).

## Example

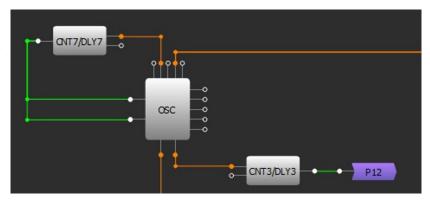
In one example, consider multiplying an input frequency of ~1 kHz by a factor of 15. The counter data CNT3 should be:

$$CD = 2 * 15 - 1 = 29$$

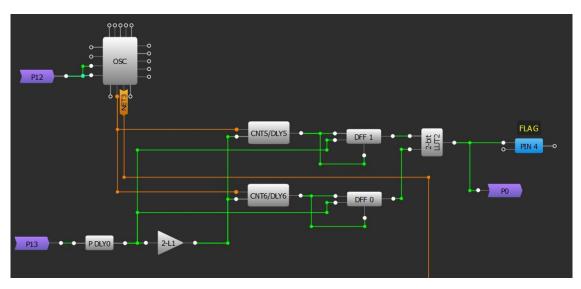
The counter period of CNT7 should be:



4. Selector



5. Multiplier settings



6. FLAG

## $T \approx [1/(100 \cdot 1000 \text{ Hz} \cdot 15)] \approx 666 \text{ ns}$

## **Experimental Waveforms**

Figures 8 through 12 illustrate the experimental waveforms.

Channel 1 (yellow/top line): PIN#12 (IN)

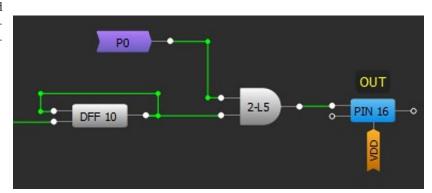
Channel 2 (light blue/2nd line): PIN#4 (FLAG)

Channel 3 (magenta/3rd line): PIN#16 (OUT)

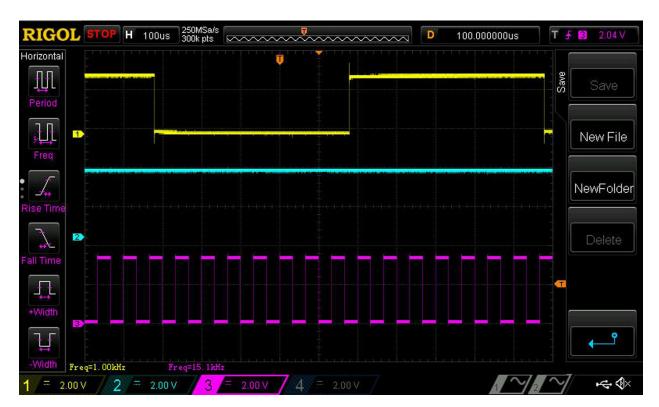
#### Conclusion

This article demonstrates how to make a frequency multiplier using a GreenPAK IC. Only a few internal blocks of the SLG46620 chip are used, leaving the bulk of the blocks available to build other circuitry. The given design is limited to an input frequency range of 0.2x to 5x the typical frequency for which the circuit was debugged (~1 kHz). The typical output frequency can't exceed 135 kHz.

Due to its size, configurability, and price, the GreenPAK provides an efficient and low-cost approach to implement a frequency multiplier.



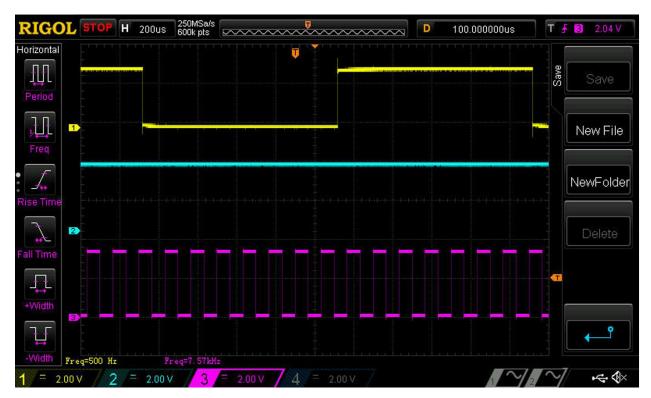
7. OUT



8. Waveform when input frequency is 1 kHz.



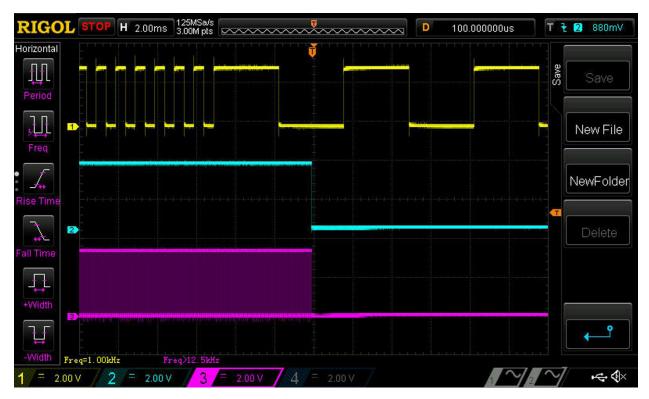
9. Waveform when input frequency is 2 kHz.



10. Waveform when input frequency is 0.5 kHz.



11. Waveform when input frequency is 6 kHz.



12. Waveform when input frequency is 150 Hz.