

Power Density in 3D Power Packaging

Power-supply designers are more frequently being tasked to deliver higher power in the same footprint they had in their last design. 3D packaging will help make this goal a reality.

New and emerging technologies for 3D packaging are being deployed at the printed-circuit-board (PCB) level. Power-density goals can be simplified with component integration into chip-scale packages that use stacking techniques, integration, transposers, and more. Advanced cooling methods will help make 3D packaging a viable option.

The latest technology innovations and cooling methods will improve power density in new designs and upgrade it in older designs. These innovations and methods, in this article, will greatly improve the power density in 3D power packaging.

Embedding and Integrating

Face up/face down

Present-day technology enables embedding of such things as active and/or passive components, magnetics, and integrated filters into the circuit board.

Texas Instruments MicroSIP was the first commercial dc-dc converter produced with the [HERMES](#) “Face down approach.” The HERMES project aims at embedding active dies, face up or face down (flip chip), and (thin) passive components inside the dielectric layers of a PCB.

Embedding magnetics

Plated through hole (PTH) and blind via (BV) are two

technologies that make it possible to *embed* (Fig. 1).

Reliability of 3D Integrated Power Packaging

Increasing power density in power electronics designs will require better cooling techniques moving forward, such as integrated cooling. Controlling temperatures of power components is crucial to device reliability and performance. However, innovative thermal management of power electronic systems is a key bottleneck to power densification.

Wirebond/Solder Die Attach vs. Sintered Interconnects

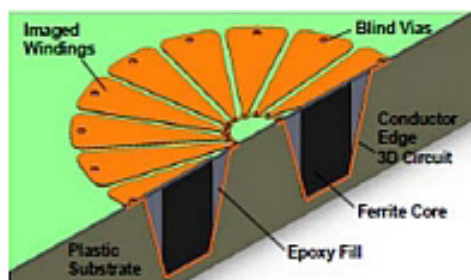
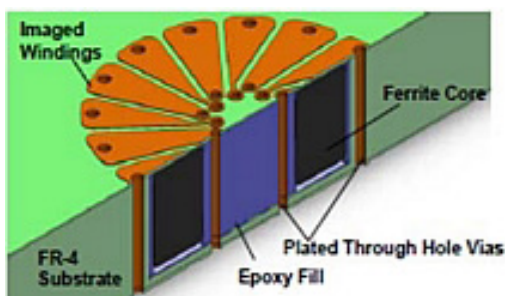
For optimum power-density reliability, traditional wirebond techniques need to move toward sintered interconnects, which would eliminate wirebond failures.

Silver sintered power devices are an alternative interconnect technology to standard solders. The technology is different from other interconnect technologies due to improved thermal and mechanical properties. A high fatigue life is achieved in testing when compared to standard solder die attach and Al wire top contacts.

Embedded components

Capacitors

There are two methods of embedding capacitors into 3D structures:



1. Plated through hole (PTH) and blind via (BV) are two technologies that can be used to embed magnetics. (Image from Reference 1)

- Embedded capacitor films
- Embedded capacitor devices

Inductors

There are two means of embedding inductors into 3D structures:

- Planar magnetics
- Deposited inductors

Cooling methods in 3D power packaging

Embedded manifold-microchannel coolers

These types of coolers can be embedded directly into the substrate or chip and will provide localized heat removal at high volumetric rates from the backside of active integrated circuits and power electronic devices (Fig. 2). They can be used in many forms; for example, single- vs. two-phase, silicon vs. ceramic substrates and different alloys, filter size, working fluid, fluid velocity, and temperature.

Force-fed two-phase manifold cooler

A series of parallel microchannels can have perpendicularly oriented manifold to distribute flow (Fig. 3). A micro-grooved surface is manufactured in single-crystal silicon carbide (SiC).

Adequate thermal isolation of power devices from one another

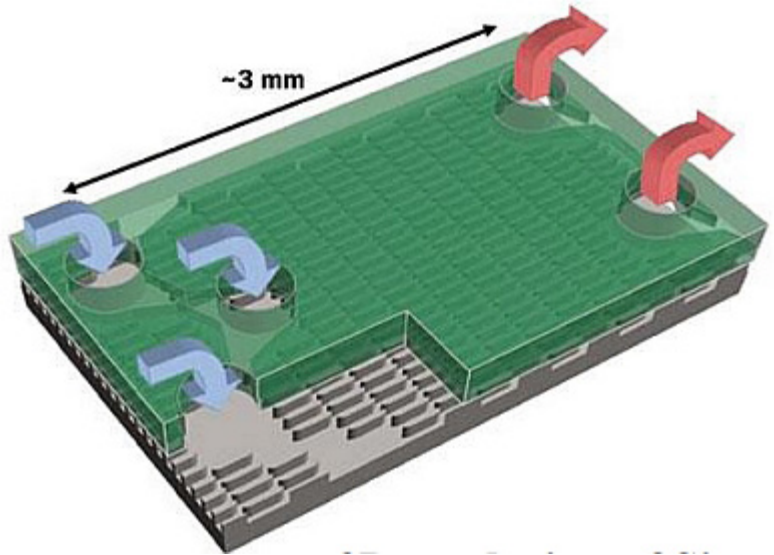
3D integrated power electronics will use new packaging technologies. The reliability of these methods for cooling is still being understood and modeled.

Fluid immersion cooling

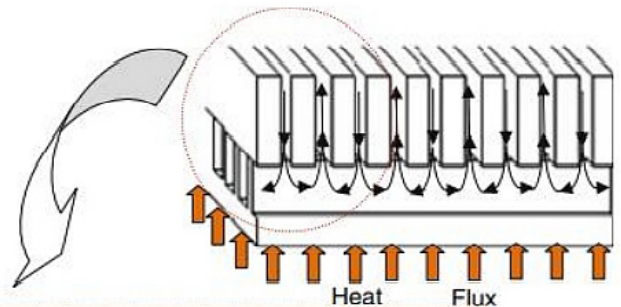
Immersion cooling has risen as a solution to overcome barriers, such as single-phase cooling, by a method of boiling a cooling fluid directly from the electronic components. This will help remove the need for most thermal interface materials and packaging constraints found in many other approaches.

State-of-the-art immersion-cooling systems employ dielectric heat-transfer liquids due to electrical considerations. This presents fundamental disadvantages related to the relatively low boiling point, low critical heat flux ($< 20 \text{ W/cm}^2$), and relatively poor thermophysical properties (e.g., thermal conductivity, latent heat, surface tension) when compared to higher performance fluids such as water. However, compromises need to be considered since water can damage electronics systems. Check out “[The Best Heat Transfer Fluids for Liquid Cooling \(boydcorp.com\)](http://boydcorp.com)” for viable heat-transfer fluid options.

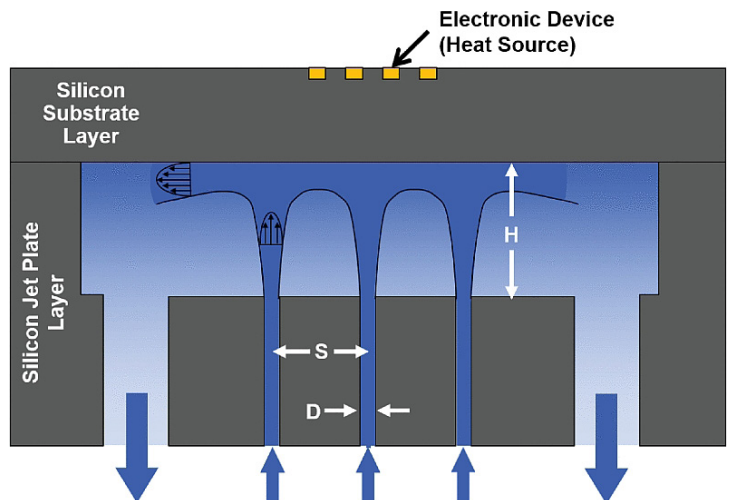
High heat transfer of microjet impingement



2. Shown is a 3D rendering of a silicon microchannel cooler. (Image from Reference 1)



3. This is a force-fed, two-phase manifold cooler. (Image from Reference 1)



4. The embedded microjet impingement is integrated within the device substrate. (Image from Reference 2)

Improving the power density of advanced electronics, and in particular gallium-nitride (GaN) high electron mobility transistors (HEMTs) in RF power amplifiers, represents a big challenge in thermal management. High-heat-transfer capability of microjet impingement can be employed to bring cooling directly to the backside of the power electronic device (Fig. 4).

High-power-density electronics device cooling loop using a liquid-metal coolant

This method employs the use of liquid gallium alloys, which have a thermal conductivity (approx. 28W/m/K) that's 40 times greater than the thermal conductivity of water.

Summary

This article has suggested some very powerful methods that designers can employ to increase power density in 3D packaging. For instance, embedding and integrating was mentioned as a good way to improve power density. Various cooling methods also were discussed as ways to boost power density. Which method is best suited for your 3D-packaging design?

References

1. [Reliability of 3D Integrated Power Packaging \(psma.com\)](http://psma.com)
2. ["Embedded Microjets for Thermal Management of High Power-Density Electronic Devices," IEEE Journals & Magazine](#)
3. Study and realization of a high power density electronics device cooling loop using a liquid metal coolant, Grenoble Electrical Engineering Laboratory (G2Elab)