Electronic Design

By FRANCESC ESTRAGUÉS, Applications Engineer,
Monolithic Power Systems, monolithicpower.com

Designing a Power Tree for an Automotive SoC

ADAS and infotainment SoCs offer increasingly higher computing power, which in turn results in higher power demands. This article discusses how to design an optimal power architecture for an automotive SoC, focusing on pre-regulator design.

Advanced driver-assistance systems (ADAS) and infotainment systems-on-chip (SoCs) continue to ramp up the computing power, leading to higher power demands. An SoC can require more than 10 different power rails, with currents ranging from hundreds of amperes to a few milliamperes. Crafting an optimal power tree for these applications isn't a trivial task. Here, we'll discuss how to design an optimal power architecture for an automotive SoC, with a focus on the pre-regulator design.

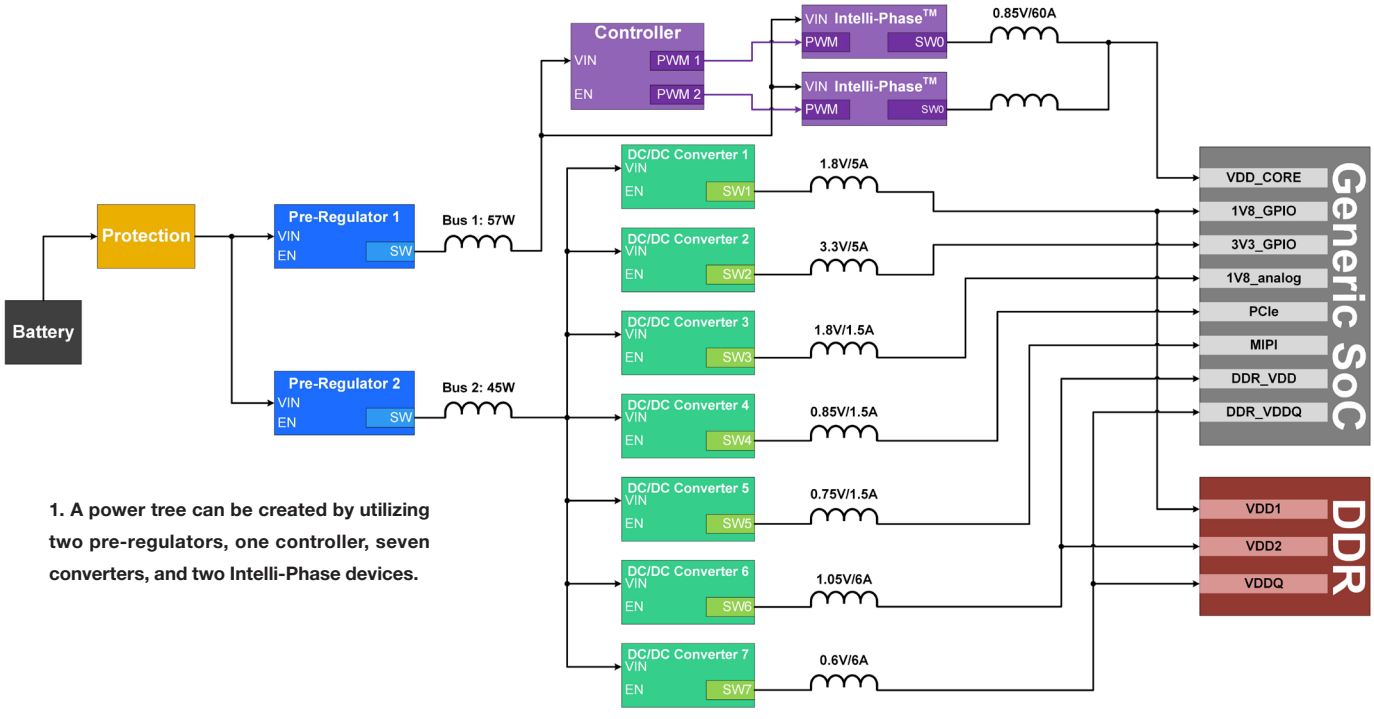
Challenges for Automotive Batteries

A 12-V battery bus in an automotive environment can experience various stressors, such as transient overvoltage (OV) and undervoltage (UV) conditions that occur during car operation. Consequently, most dc-dc integrated circuits (ICs) designed to operate from a PC's 12V bus aren't well-suited for automotive applications.

A pre-regulator is required to prepare the field for the low-voltage dc-dc ICs. This pre-regulator should generate a clean bus (typically 5 or 3.3 V) from which the core voltage regulator (VR) and the other converters operate.

SoC Requirements

In the early stages of development, the SoC power requirements typically provide each rail's voltage and current ratings, as well as the expected transient currents that the



1. A power tree can be created by utilizing two pre-regulators, one controller, seven converters, and two Intelli-Phase devices.

Rail Name	Voltage (V)	Current (A)	Transient Load (A)	Slew Rate (A/µs)	Voltage Tolerance (1) (%)	Notes
VDD_CORE	0.85	60	40	40	3	
1V8_GPIO	1.8	5	2.5	2.5	5	
3V3_GPIO	3.3	5	2.5	2.5	5	
1V8_analog	1.8	1.5	0.75	0.75	5	From a low-noise DC/DC converter
DDR_VDD	1.05	6	3	3	3	
DDR_VDDQ	0.6	6	3	3	5	
PCIe	0.85	1.5	0.75	0.75	5	From a low-noise DC/DC converter
MIPI	0.75	1.5	0.75	0.75	5	From a low-noise DC/DC converter

system must be prepared to support. It's the power architect's job to translate this information into a comprehensible, high-level diagram from which to start the hardware design *(Fig. 1)*.

Table 1 shows an example of SoC power requirements. Note that the voltage tolerance includes the converter's dc accuracy, load transient response, and IR drop.

Note that there are two pre-regulators to limit the output power for each converter to about 50 W. By implementing two pre-regulators, designers can have more options for IC selection.

Selecting the Pre-Regulator Topology

The first step when designing the pre-regulator is to determine its topology. Depending on the required operating conditions, this regulator can be a buck converter, buck-boost converter, or a combination of buck and boost converters.

If the system must operate during a warm-crank event, but it can turn off briefly during a harsher cold-crank event, it's recommended to select a buck-converter topology for improved cost and efficiency. If any circuit needs a voltage exceeding 5 V during the warm-crank event, a post-boost converter can be added to ensure that the circuit is supplied with the required voltage.

Otherwise, if the circuit must operate under a severe cold-crank event as well, choose a buck-boost converter to guarantee that the system operates under all potential conditions. Note that a buck-boost converter is typically more expensive and less efficient than a simpler buck converter. For this design example, a buck converter was selected.

Setting the Bus Voltage

Once the topology is selected, the designer must consider the bus voltage. This bus voltage—typically 3.3 or 5 V—supplies all downstream converters. Most low-current dc-dc ICs can operate from up to 5.5 V, so either voltage would work. However, solutions with a controller and an Intelli-Phase converter must operate from a ≥5-V bus.

The bus voltage is typically selected to optimize cost, as stepping down directly to 3.3 V can sometimes reduce the number of required converters. However, it also requires a higher output current than when the voltage is converted to 5 V.

Each pre-regulator's power rating is the sum of its downstream converters' output power when the efficiency coefficient is applied. For simplicity, an 89% efficiency can be assumed for all converters. The power for pre-regulator 1 ($P_{PRE\text{-}REG1}$) can be calculated with Equation 1:

$$P_{PRE\text{-}REG1} = \frac{VxI}{\eta} = \frac{0.85x60}{0.89} = 57.3\ W \quad (1)$$

The power for power regulator 2 ($P_{PRE\text{-}REG2}$) can be estimated with Equation 2:

(see equation 2 below)

$$P_{PRE\text{-}REG2} = \frac{\sum_1^7 V_n x I_n}{\eta} = \frac{1.8x5+3.3x5+1.8x1.5+0.85x1.5+0.75x1.5+1.05x6+0.6x6}{0.89} = 45.5\ W \quad (2)$$

Then calculate the output current for each pre-regulator. Calculate pre-regulator 1's output current ($I_{PRE\text{-}REG1\_5V}$) with Equation 3:

$$I_{PRE\text{-}REG1\_5V} = \frac{P}{V} = \frac{57.3}{5} = 11.5\ A \quad (3)$$

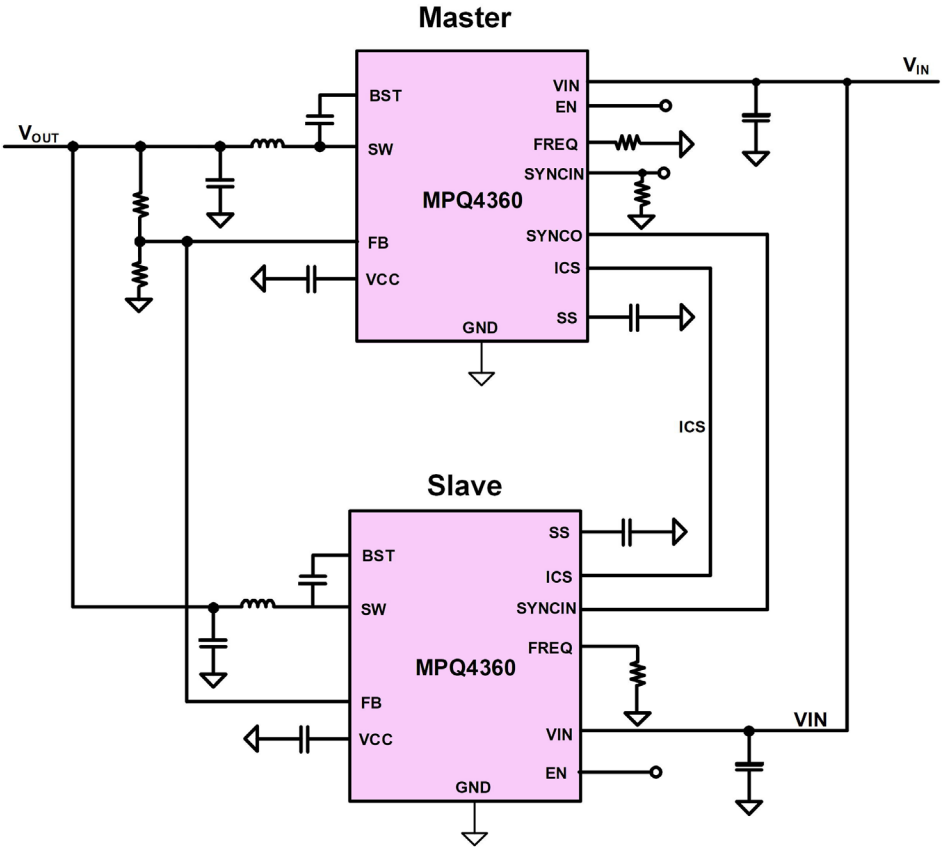
For pre-regulator 2, estimate the output current using both for the 3.3-V bus voltage option ($I_{PRE\text{-}REG2\_3.3V}$) using Equation 4:

$$I_{PRE\text{-}REG2\_3.3V} = \frac{P}{V} = \frac{45.5}{3.3} = 13.8\ A \quad (4)$$

For pre-regulator 2, estimate the output current using both for the 3.3-V bus voltage option ($I_{PRE\text{-}REG2\_5V}$) using Equation 5:

$$I_{PRE\text{-}REG2\_5V} = \frac{P}{V} = \frac{45.5}{5} = 9.1\ A \quad (5)$$

Since this system's power rating is high, a 5-V bus voltage



2. Two MPQ4360-AEC1 devices can operate in parallel to achieve 12 A of output current.

allows for a lower output current than a 3.3-V bus voltage. It's recommended to choose a 5-V bus voltage so that designers can select a less complex dc-dc converter.

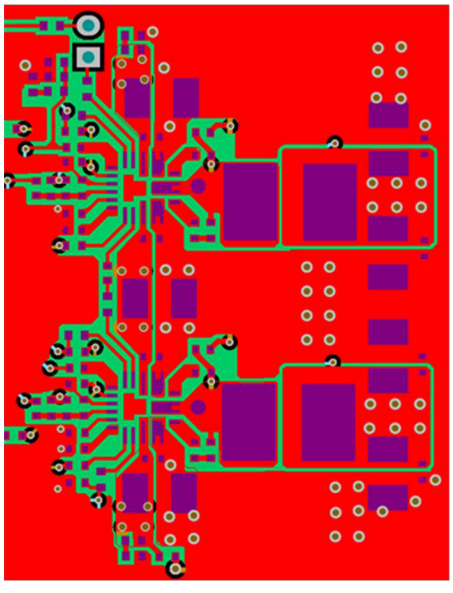
Selecting the IC

Once the topology and output load have been determined, the designer should select the pre-regulator IC. This IC must support a 42-V input voltage for load dump conditions and be able to operate down to 6 V during warm-crank conditions. In addition, the output load capability should be ≥11.5 A, or two parts should be able to operate in parallel up to that current. Both pre-regulators can use the same IC since the power level is similar.

The MPQ4360-AEC1 is a synchronous buck converter with a current rating of 6 A. It can operate in a multiphase configuration to achieve 12 A of output current. The interleaved multiphase operation reduces the electromagnetic emissions and allows for smaller components, which provides the benefit of a smaller PCB layout compared to a solution using a controller and discrete FETs.

This device also has a very low 22-µA quiescent current (I_Q), which makes it well-suited for automotive applications. *Figure 2* shows two MPQ4360-AEC1s operating in parallel.

Figure 3 illustrates an example of the PCB layout for the MPQ4360-AEC1 in dual-phase operation. The approximated solution area is 750 mm^2.



3. Paralleling two MPQ4360-AEC1 devices can create a tiny solution for space-constrained applications.

System Protections

The battery bus can experience a hazardous reverse supply voltage. If the system isn't protected in this scenario, all of the devices can be damaged. To prevent reverse-current flow, a diode is typically added to the input line. However, diodes have a forward voltage (V_F). As current flows through the diode during normal operation, V_F creates a power loss.

The designed SoC system has a power rating of >100 W; for a 12-V battery, this translates to an input current that can exceed 8 A. But 8 A is too large for a simple diode—and even when using a Schottky diode with a V_F of 0.3 V, the power loss would exceed 2.4 W. A standard alternative is to use a P-channel MOSFET to block the reverse current, but these MOSFETs may not be able to protect the IC from high-frequency ac currents in a sufficient timeframe.

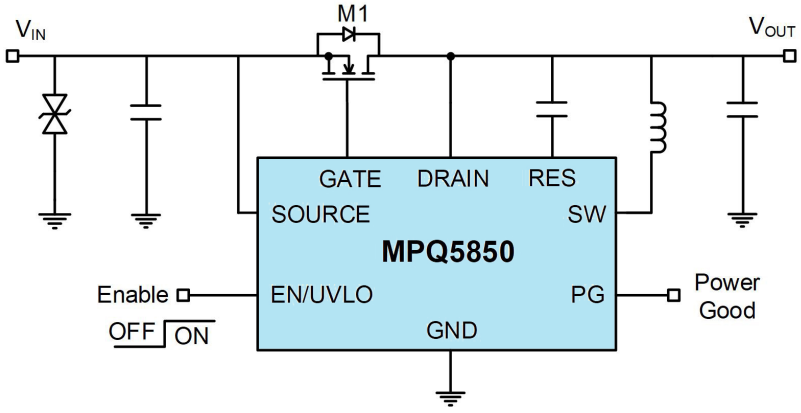
To that end, the MPQ5850-AEC1 is an ideal-diode controller that can protect the system from reverse-current flow. *Figure 4* shows how the MPQ5850-AEC1 controls an N-channel MOSFET with a strong gate-driving capability to quickly block any reverse-current flow. This provides reverse-current protection with minimal power loss.

Figure 5 shows the updated power tree once the pre-regulator and protection device are selected.

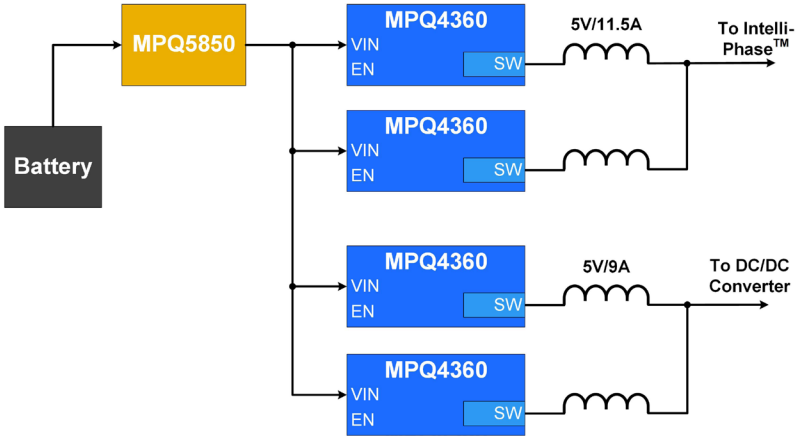
Conclusion

Selecting the correct pre-regulator for an ADAS system isn't an easy task. Using an IC that allows its output to be paralleled in a multiphase topology makes this design more straightforward. For example, the scalable solution using the MPQ4360-AEC1 and MPQ5850-AEC1 enables each rail to meet its required output current in a small area, while reducing BOM cost.

For additional reading, refer to this article to learn more about automotive transients.



4. An N-channel MOSFET enables the MPQ5850-AEC1 to block reverse-current flow.



5. The MPQ5850-AEC1 and MPQ4360-AEC1 contribute to an efficient pre-regulator and protection power tree.