Electronic Design

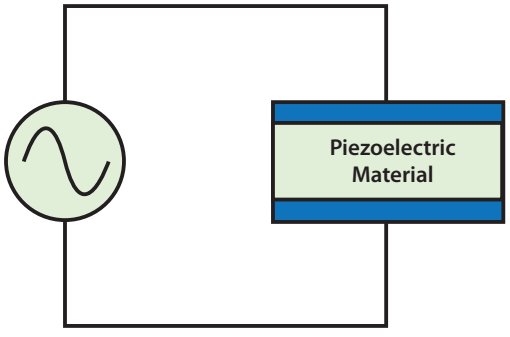
By RICK NELSON, Contributing Editor

The Connected World Marches to the Beat of BAW Technology

Sponsored by Texas Instruments: Bulk-acoustic-wave resonators can replace quartz-crystal oscillators to enhance performance and reliability while minimizing supply-chain issues.

Devices ranging from microcontroller units (MCUs) to field-programmable gate arrays (FPGAs) permeate our connected world. To operate properly, such devices require clocks to synchronize the data they process, transmit, and receive.

Bulk-acoustic-wave (BAW) technology enables the fabrication of compact, precise, reliable clocks with programmable frequencies, eliminating the need to stock multiple crystals operating at different fixed frequencies. BAW resonators have a key and growing role to play in ensuring seamless communications between mobile and Internet of Things (IoT) devices and cloud-computing resources.



1. A BAW resonator includes a piezoelectric material sandwiched between two electrodes.

MEMS-Based Resonators

A BAW resonator is a microelectromechanical-system (MEMS) that consists of piezoelectric material sandwiched between two electrodes *(Fig. 1)*. This material can convert electrical energy to mechanical-acoustical energy, producing reliable oscillations that enable a high-frequency clock output. A BAW resonator enables Texas Instruments' CC2652RB SimpleLink MCU to operate without an external crystal oscillator.

The MCU's integrated resonator reduces its footprint and minimizes bill-of-materials (BOM) costs without compromising latency, and it offers ±40-ppm frequency stability across the full operating-temperature and operating-voltage ranges. In addition, the 2.4-GHz multiprotocol MCU offers ultra-low jitter and phase noise to meet the clock requirements of various wireless-communication standards.

TI also integrates BAW technology into its LMK6C low-jitter, high-performance, fixed-frequency oscillator. It delivers enhanced jitter performance and improved reliability in terms of vibration, shock, temperature stability, and reliability.

On top of that, the technology finds use in TI's LMK05318 high-performance network synchronizer clock device, which provides jitter cleaning, clock generation, and advanced clock monitoring to meet the timing requirements of communications-infrastructure and industrial applications. The ultra-low jitter and high power-supply noise rejection (PSNR) of the device can reduce bit error rates (BERs) in the high-speed serial links that traverse the connected world.

BAW vs. Quartz

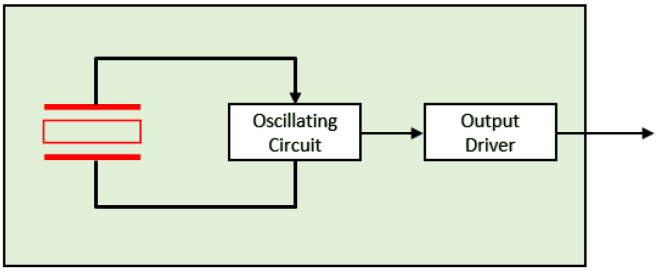
The new BAW technology competes with the venerable quartz-crystal oscillator, which has dominated the timing reference market for more than a century. But BAW offers significant advantages: It consumes less power, permits smaller system designs, and simplifies system integration while offering similar or better performance than quartz.

A review of quartz resonators helps illustrate some of their drawbacks in comparison with BAW implementations.

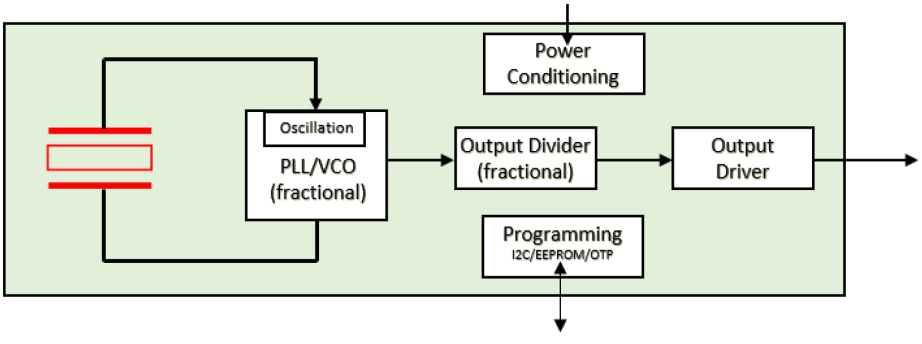
Figure 2 illustrates one way of implementing a quartz oscillator—combining a quartz crystal, oscillating circuit, and output driver.

The setup is simple and exhibits quick startup time, but its frequency depends completely on the crystal chosen—changing the frequency requires changing the crystal, so you would need to stock different batches of crystals for every frequency of interest. In addition, such an oscillator rarely operates at a fundamental frequency beyond about 50 MHz, because higher frequency crystals are difficult to manufacture.

The approach shown in *Figure 3* overcomes some of these drawbacks. Here, the crystal serves as a reference to a phase-locked loop (PLL), which can generate frequencies in the gigahertz range. A fractional output divider, programmable via an inter-integrated circuit (I^2C) interface with programming information stored in electrically erasable programmable read-only memory (EEPROM), generates the desired frequency.



2. A simple quartz oscillator's output frequency depends on the choice of crystal (red).



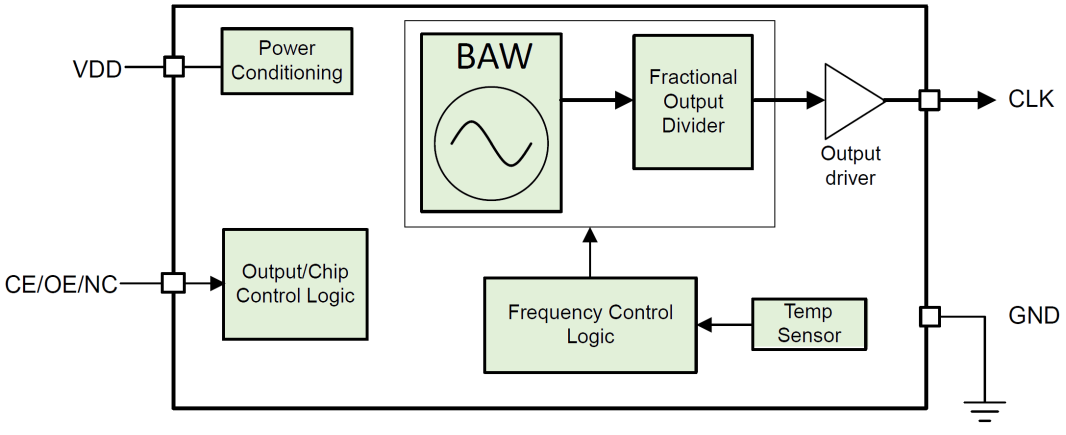
3. A fractional output divider enables programming of the output frequency.

However, this approach requires more core blocks than the one in *Figure 2*, leading to a larger package size and higher power consumption. In addition, startup time is slow because the PLL requires 10 ms or longer to calibrate and lock.

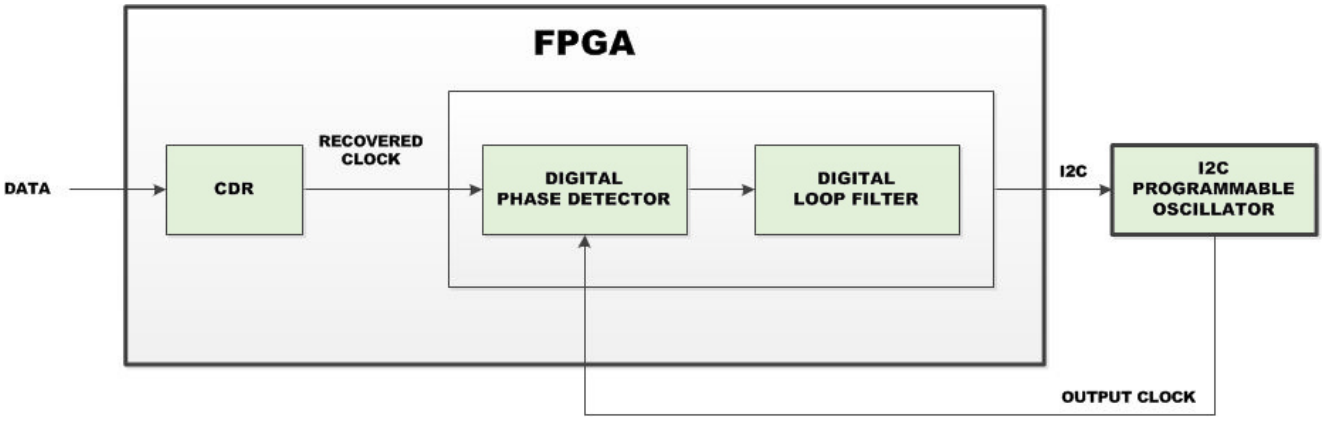
Figure 4 shows an oscillator with an integrated BAW resonator replacing the external crystal. As with the *Figure 3* circuit, a fractional output divider generates the desired frequency based on a programmed value stored in memory. Texas Instruments can fabricate such devices in four- or six-pin packages (for single-ended and differential outputs, respectively).

Each such device incorporates its circuitry on a base die designed in a deep-submicron process technology. A co-located sensor continuously monitors temperature variations, and a signal-processing algorithm uses calibration coefficients stored in nonvolatile memory to keep frequency within a ±10-ppm budget. The low-jitter low-power fractional output divider enables temperature compensation to occur with minimal impact on phase jitter. In addition to temperature stability, the device offers good phase-noise performance, with the differential-output version limiting jitter to 125 fs.

The BAW-based device includes internal low-dropout regulators (LDOs) to provide improved PSNR. It also meets MIL-STD-2007 Condition A and MIL-STD-2002 Condition A requirements for shock and vibra-



4. The BAW oscillator with single-ended output fits in a four-pin industry-standard package.



5. A digitally controlled programmable oscillator serves in a CDR circuit implemented in an FPGA.

tion, with frequency deviation due to vibration limited to about 1 ppb/g. That's nearly an order of magnitude improvement compared with quartz oscillators.

Clock Generation for FPGAs

FPGA designs often require flexible, high-performance oscillators or clock-generator ICs to provide one or more clock inputs. An FPGA's serializer/deserializer (SERDES) transceiver typically relies on external reference clocks with low integrated root-mean-square (RMS) jitter to minimize transceiver bit errors. BAW resonators can readily generate the frequencies required for FPGA designs.

For applications that require recovery of a clock signal from a serial data stream, a serially programmable resonator can serve as a digitally controlled oscillator in an FPGA-based clock-data recovery (CDR) circuit.

As shown in *Figure 5*, FPGA logic implements a digital phase detector and digital loop filter. The latter writes a control word into the programmable oscillator registers through an I^2C interface. The oscillator then adjusts its output frequency based on this loop-filter control word. The frequency adjustment required to track the recovered clock is typically measured in parts per million (for example, less than ±50 ppm from nominal).

Conclusion

BAW resonators offer the flexibility to augment applications ranging from IoT edge devices incorporating MCUs to high-performance systems employing FPGAs. Versions with a serial programming interface and onboard EEPROM provide the flexibility to support multiple frequencies and streamline the entire product lifecycle. Compared with quartz-crystal-based resonators, BAW resonators combine high performance, reliability, and availability with short lead times and simplified supply-chain management.