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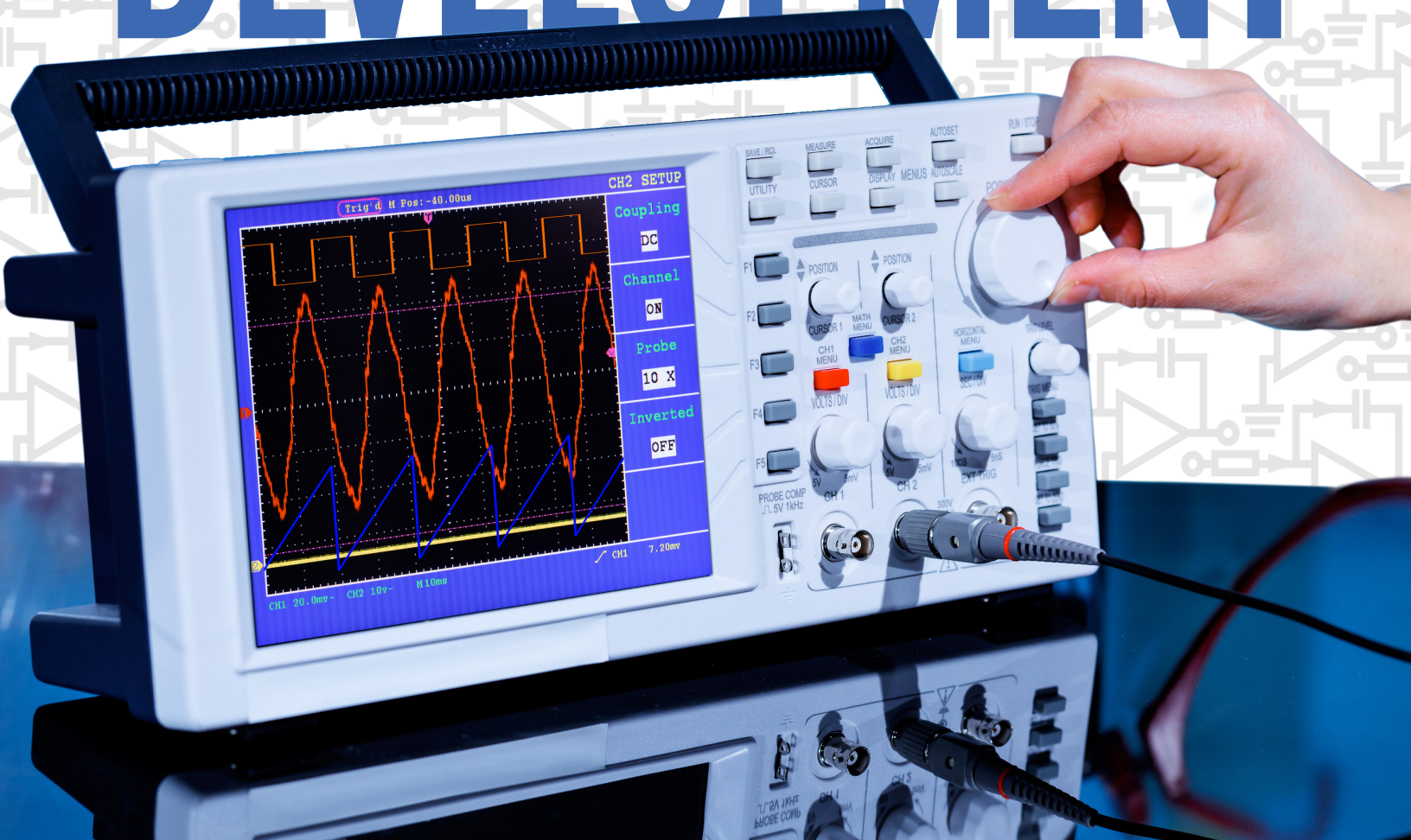
What You Need to Know About SIGNAL PATH DEVELOPMENT



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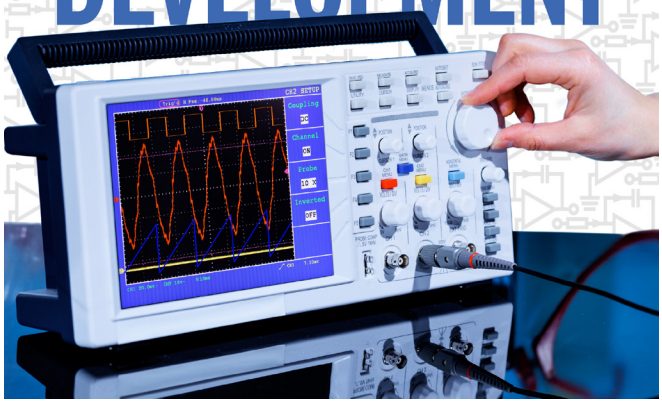
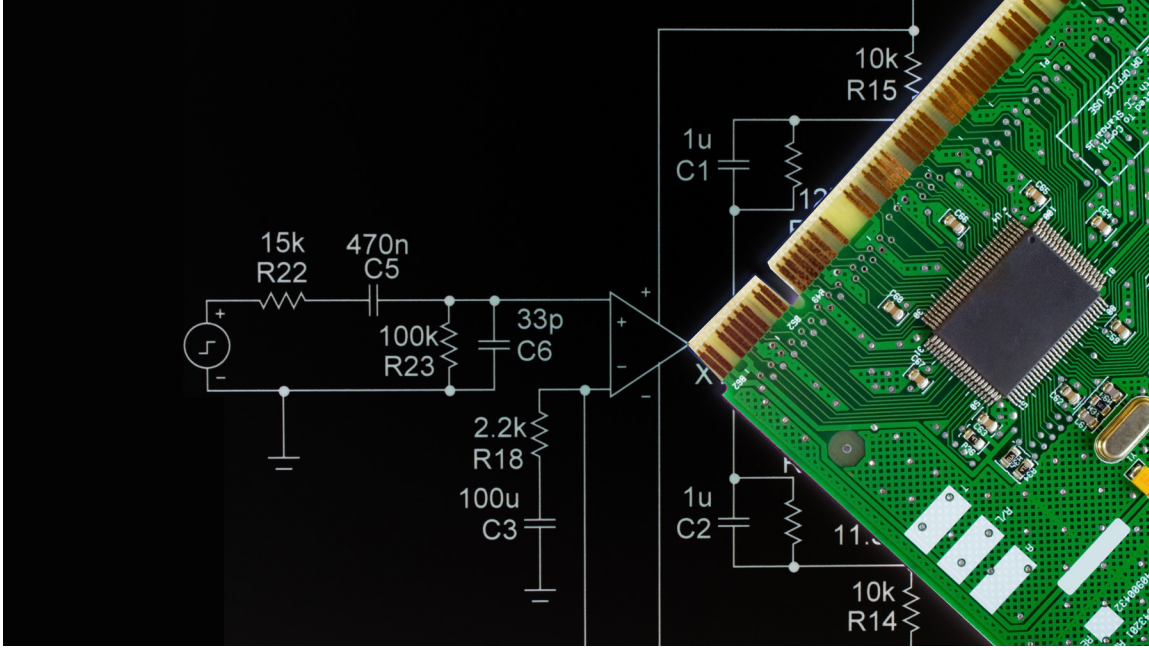


CONTENTS

ANALOG SIGNAL PATH DESIGN using op amps and/or FDA's continue to be at the core of many data acquisition or signal generator systems. The available vendor solutions span a >50yr period of vigorous developments by countless IC designers, applications, and test engineers across numerous companies. How does a new, or even experienced, analog designer absorb this mountain of data and design options to arrive at a credible (or possibly even incredible) solution.

Michael Steffes
Analog Signal Path Consultant

Compressing the common issues and confusions observed over decades of design-in support, these 3 articles review 1st the most common oversights and confusions that plague new designers, then highlight the key inconsistencies across the 100's of supplier datasheets, and finally highlight some useful new insights and devices for the analog designer that have likely not found there way back into textbooks yet.



CHAPTER 1:

Three Major Design Pitfalls Plaguing New Analog Signal-Path Designers

MICHAEL STEFFES, Analog Signal Path Consultant

Wouldn't it be great to not repeat the same amplifier application errors many new designers fall into? Read on to head off these common confusions and oversights.

Having been on the receiving end of designer queries from 1985 forward, there are some common oversights and misunderstandings that show up regularly. These essentially fall into three areas:

1. Not considering the actual operating voltage range on the I/O or internal pins of the device being used.
2. Misunderstanding the elements that contribute to an output dc offset or drift error.
3. Accidentally building an oscillator (or even worse, a nominally stable design that slips over into oscillation over production and/or temperature ranges).

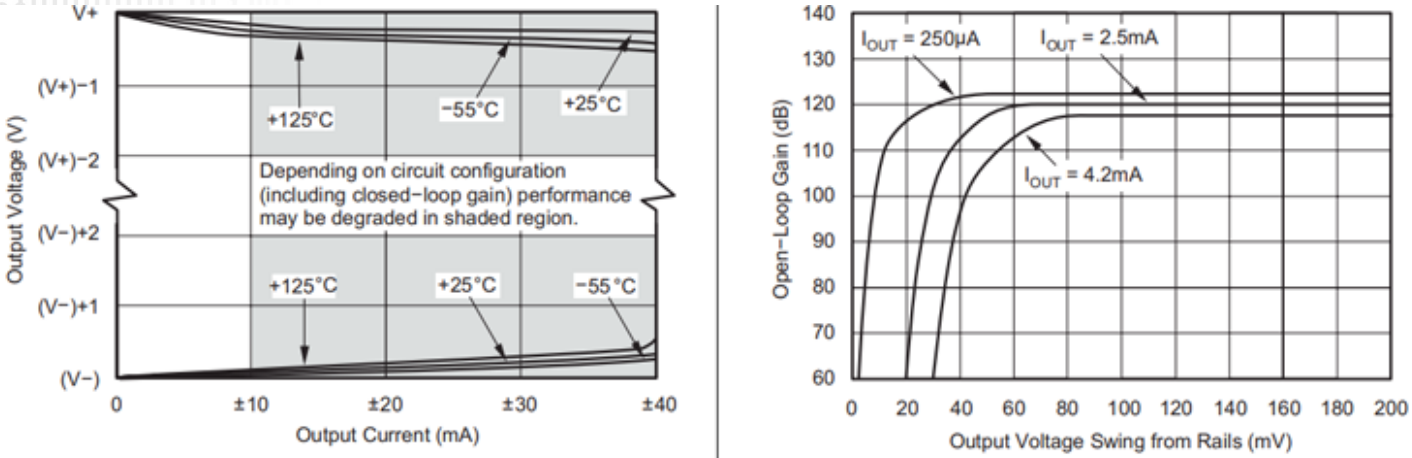
Running Into I/O Range Limits with Op Amps, FDAs, and INAs

The evolution of op amps began with very simple designs requiring considerable headroom to the supply voltages in both the input pins and the output pin. This carried over into the early fully differential amplifier (FDA) and instrumentation amplifier (INA) developments.

Over time, the need to provide more of the available supply voltage range on the I/O pins first led to rail-to-rail output (RRO) designs, then added negative rail input (NRI) designs, and more recently rail-to-rail input/output (RRIO) designs. These each come with compromises in the internals to the device.

Many single-supply designs will select at least a RRO and NRI device and then expect the device to operate with no input signal with the V+ and output pins at 0 V. All RRO devices require some small headroom to the supplies to operate linearly.

While that may be as low as 10 mV, it's still not zero. Asking the op amp to perform as expected with 0-V input will usually cause performance problems. Most NRI devices can



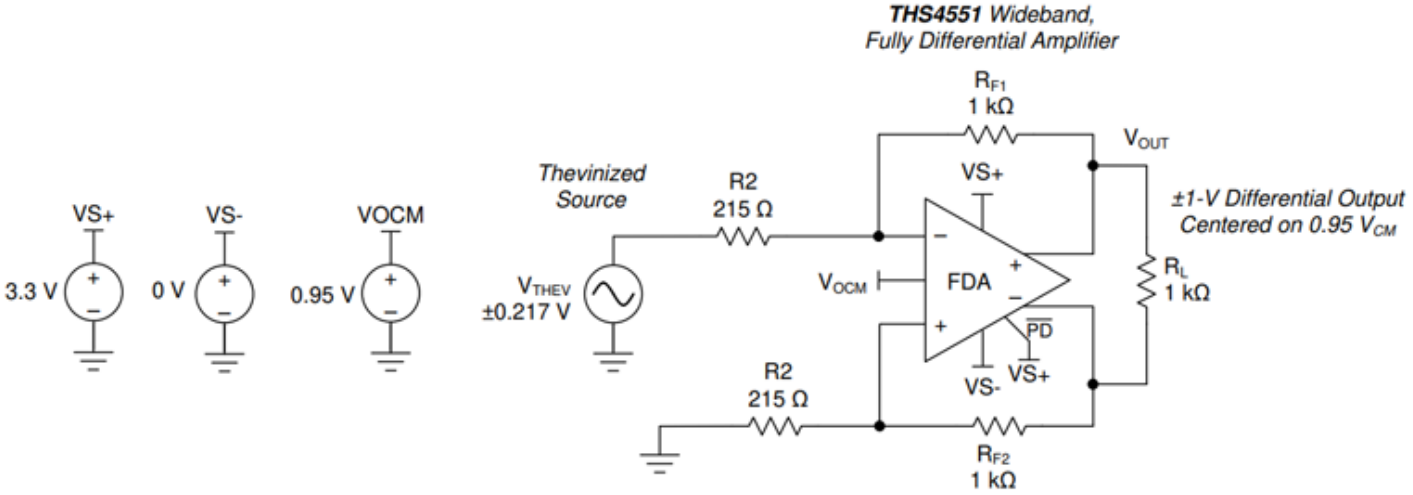
1. This example output swing "Claw" curve shows the added headroom with output current demand and the open-loop gain reduction near the supply's warning of a loss of linearity.

actually operate slightly below the negative supply; therefore, a 0-V input on a single-supply design usually will not hit an "input" limit.

Another source of confusion has been the long-term evolution of how this "headroom" is specified. Early devices (still available) talk about a ground centered maximum ±VOUT swing on a bipolar supply. While accurate, it's much more useful to think in terms of required headroom at the output (and input) to each supply voltage being used. Most early devices specified no load or a specified load for this swing.

The required headroom always increases as the demand escalates for more output current. This, and the open-loop gain reduction near the supplies, are captured in more recent op amps as shown in the curves of **Figure 1** from the OPA350 datasheet (OPAx350 datasheet). While a true swing to ground is required in a single-supply design, some designs apply a fixed −0.23-V bias generator like the LM7705 (LM7705 datasheet).

The first commercial FDA—the AD8138—emerged in 1999. Subsequent developments have pushed towards extreme dc precision (and speed with low power) in mainly NRI and RRO designs like the THS4551 (THS4551 datasheet).



2. Input common-mode swing analysis for a single-supply dc-coupled application example.

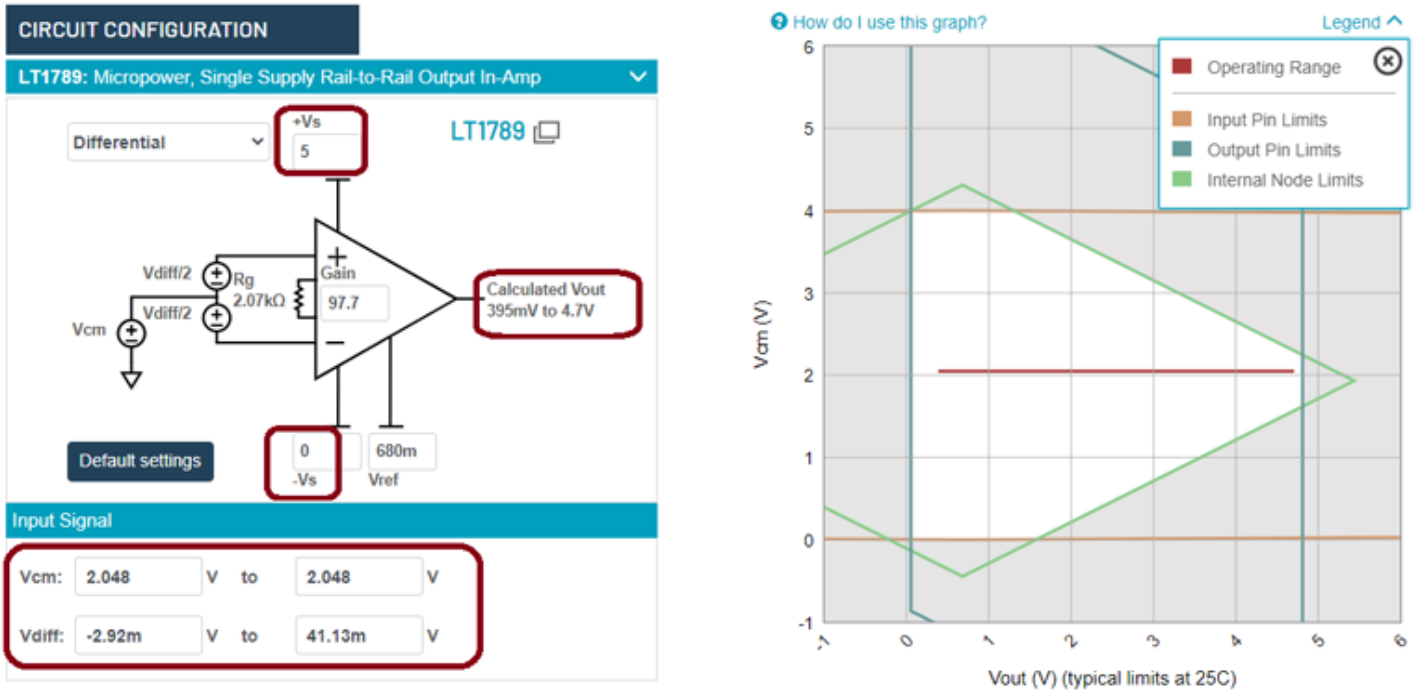
One common confusion when applying these modern FDAs is that a single-supply design can, in fact, take a dc-coupled bipolar input and operate all I/O pins with enough headroom on a single supply. The key here is that the common-mode (CM) control loop will force a dc level-shifting current back through the input resistors to level-shift the input CM voltage across the two inputs to operate above ground, even with a bipolar input signal. This effect is illustrated in **Figure 2**. Any FDA circuit can reduce the input networks to Thevenin equivalents as shown in Figure 2. A good design will have equal feedback resistors and equal Thevenin impedances looking back from the two inputs to a source and ground (or low-impedance reference voltage).

The easiest way to see that the input CM voltages are above ground is to consider the lower output side of the FDA in Figure 2 dividing back to ground. If the output is correctly swinging ±0.5 V on each side around the stated 0.95-V CM voltage, the 0.45- to 1.45-V absolute swing on that lower output will divide back to the lower input pin as 0.177 × 0.45 V to 0.177 × 1.45 V equal to 80 to 256 mV.

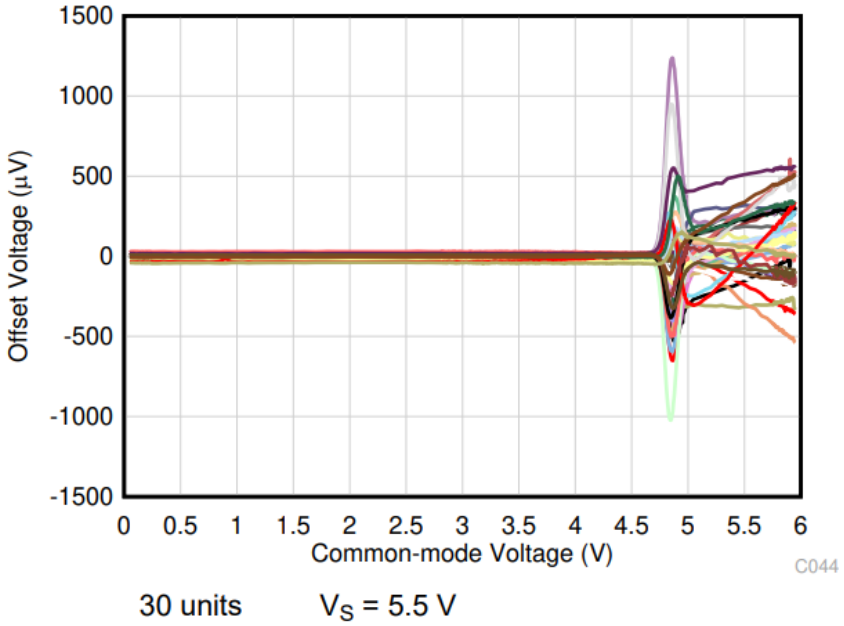
Yes, the input CM voltage moves with the full-scale swing of the input signal but never goes below ground. Actually, since the outputs can't go below ground, that feedback signal to the lower summing junction can't swing below ground. The FDA differential loop forces the error voltage across the inputs to zero. Thus, the input pins move together for a single-ended input to differential output application.

A very popular solution in precision industrial applications is the instrumentation amplifier (INA). These typically present two high-impedance inputs with a settable differential gain to a single-ended output stage. Such an output often includes a reference voltage input that independently sets an output dc level separate from the input-signal-induced output swing.

Those all have specified input and output headrooms much like an op amp or FDA device. They also often have internal swing limits not directly observable in application or simulation.



3. Diamond plot tool setup for a thermocouple application showing valid operating range.



4. The input crossover network shows a large offset voltage step near the positive supply for the OPA396 precision CMOS RRIO op amp.

These hidden limits have tripped up many a design engineer.

Several INA suppliers have developed tools to expose these limits in application. One is the instrumentation amplifier diamond plot tool (ADI Diamond Plot Tool for INAs). This tool allows designers to enter their intended input conditions and a desired gain and reference voltage, along with a candidate device, and immediately expose internal and external clipping issues.

Figure 3 shows an example drawn from an actual thermocouple design where the input CM voltage is fixed at 2.048 using a single 5-V supply on the LT1789 INA. If the red line in the diamond plot is completely within the white area, unclipped operation is assured.

Designer Oversights in Assessing Output DC Precision and Drift

The calculations for output dc error and drift are well-trodden trails in academic and vendor material. Several detail issues continue to trip up new (as well as experienced) designers with the vast proliferation of op-amp and FDA solutions.

Classic bipolar input op amps and FDAs usually offer a well-matched input bias current error if it's a voltage feedback amplifier (VFA). It's effect on an output dc error can be reduced using a "bias current cancellation" resistor solution to reduce the output dc error to the offset current at the inputs (mismatch specification) times the feedback resistor value. For voltage-feedback op amps, this simply requires you to match the dc impedance looking out the V+ pin to the parallel combination of the feedback and gain resistors on the inverting side.

But where does this actually work—and not work? It will always work with simple NPN or PNP input stages having matched bias currents. Some very-low-bias-current bipolar input devices use cancellation currents into the input pins. If so, the offset currents aren't as low as for the simpler input-stage designs. Bias currents are never matched for CMOS or JFET input devices, so designing for bias-current cancellation is a waste of time; lower R's on the V+ pin are usually desirable to reduce added noise from those resistors.

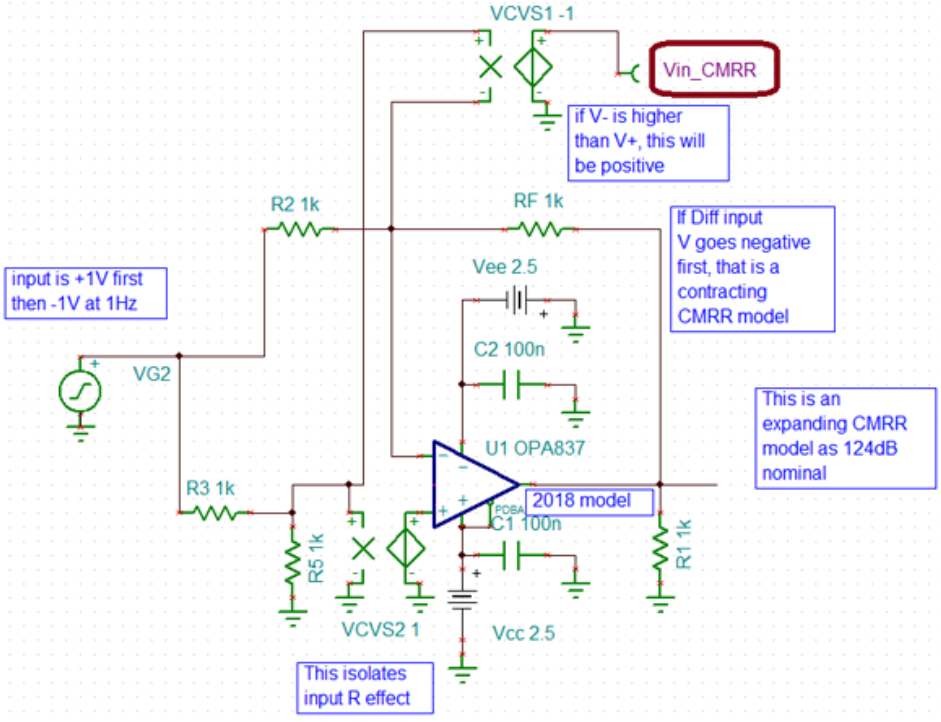
Some of the very lowest input offset voltage and drift VFAs emerged with the chopper-input types of devices. These chopper-, and trimmed non-chopper-input, CMOS devices provide sub-10-µV input offsets with very low drift. Later developments added rail-to-rail

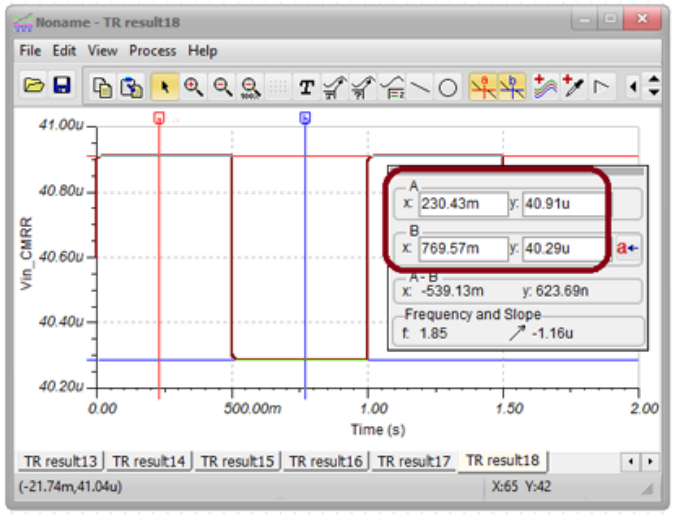
input (RRI) options using crossover networks at the input to pass control between the CMOS device types. Zero-crossover RRI types include an on-chip boost regulator to provide enough supply voltage for the input stage to get RRI without a crossover network, like the OPA328 (OPA328 datasheet).Those types of RRI devices with a crossover region will show a discontinuity in the input offset voltage as control is passed across the CM input range of the op amp. Many designers have been tripped up by this, where simply avoiding that area of the input CM might have been possible.

Figure 4 shows a good example from the recent OPA396 RRIO CMOS precision op amp (OPA396 datasheet), a non-chopper device quoting a maximum input offset of 100 µV. This gain of 1 plot clearly shows the large step in input offset voltage near the positive supply. This is easily avoided by operating with a small non-inverting gain or running inverting mode with fixed bias on the V+ pin well below this crossover.

The very best input-drift VFA op amps use a chopper-input structure. Those intrinsically need an internal switching clock that then shows up in the input current noise spectrum. Though this often isn't shown, it's usually there. Whether this effects the accuracy in the application depends on many things, but at minimum it's prudent to plan on at least a post-RC filter well below that chopping frequency to filter that off.

It's also prudent for chopper-input op amps to design for source matching as in dc bias-current cancellation. This will reduce the higher-frequency output noise due to the chopper-input current spikes ("Reducing Chopper Input Artifacts" article). Some, but not all, chopper-input op amps report that chopping frequency.





5. Simulation to test the effect of input CM swing on input offset voltage in the OPA837 model.

CMRR and PSRR

The earliest op-amp literature spent quite some time discussing the common-mode rejection ratio (CMRR) and power-supply rejection ratio (PSRR) effects on output error terms. Those usually end up showing a plot over fre-

quency that's almost always a designer simulation as the measurement is nearly impossible.

Here, only the dc values are of interest for output dc error concerns. The PSRR gets confused in the datasheets, sometimes showing the supplies moving together—but that's the same thing as a CMRR test. ATE flows move only one supply at a time to extract out an apparent shift in the input Vos voltage. These are often assumed to have a bipolar distribution in adding to the other dc error terms to get full output dc error band.

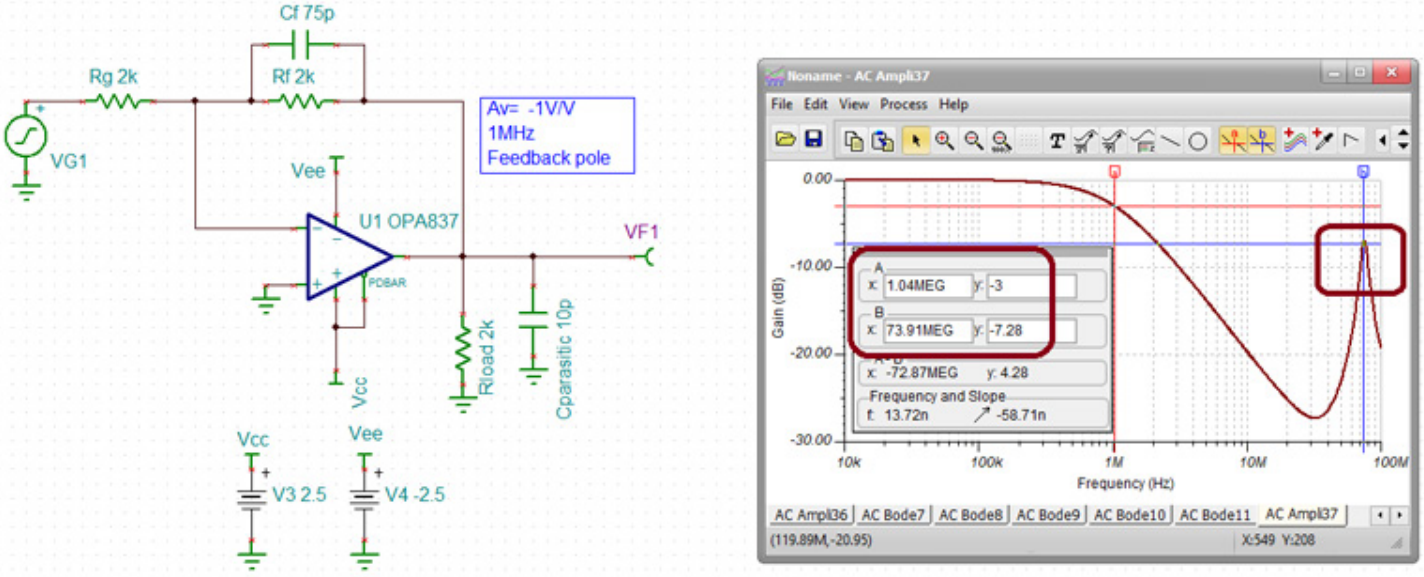
For typical single-supply designs with say a ±10% supply tolerance for a +5-V design, such an error term for modern devices is very small. Typical PSRR numbers are 110 dB or greater, so ±0.5-V supply shift in production maps to a ±1.6-µV expansion in the input offset span using a 110-dB specification.

CMRR has been presented as a shift in the input offset voltage as the CM input voltage travels across the available input span. In fact, all models and ATE data show this as a gain error term. Since the error is dependent on the input CM level, why would it be a static dc error when in fact it's more like the LG/(LG+1) gain error (where LG is the loop gain, the Aol/(noise gain)). Often, this CMRR gain error is on same order or smaller than the Aol at a gain of 1, and it becomes even less significant at higher noise gains as that LG term becomes the dominant gain error.

A simple simulation (**Fig. 5**) can easily illustrate what the model is producing. Here, the precision OPA837 (OPA837 datasheet) is set up with four equal resistors in a classic CMRR test. The output should be very close to zero swing, but here the input offset voltage is probed showing a very small 0.62-µV p-p amplitude square wave (around the nominal 40.6-µV offset voltage in the model) for a 1-V p-p CM input swing at the V+ input pin. Here a dependent unity-gain voltage buffer was inserted to isolate the V+ pin input resistance from the four-equal-resistor test setup.

The polarity indicates this model is showing a very small expansion in the gain due to CMRR effects. This 124-dB CMRR level will in practice combine with any gain error introduced by the LG/(LG+1) term. It's not clear that this expanding gain effect in the OPA837 model is matching the physical device.

Both expanding and contracting CMRR effects can be found using different op-amp



6. Inverting gain of –1 V/V with the OPA837 shows marginal stability with the feedback bandlimiting capacitor.

models in the test circuit of Figure 5. Holding a fixed (non-zero) input CM voltage (as in an inverting op-amp design) will add a fixed CMRR error contribution to the total input Vos calculation.

Ignore Nominal Design Phase Margin at Your Peril

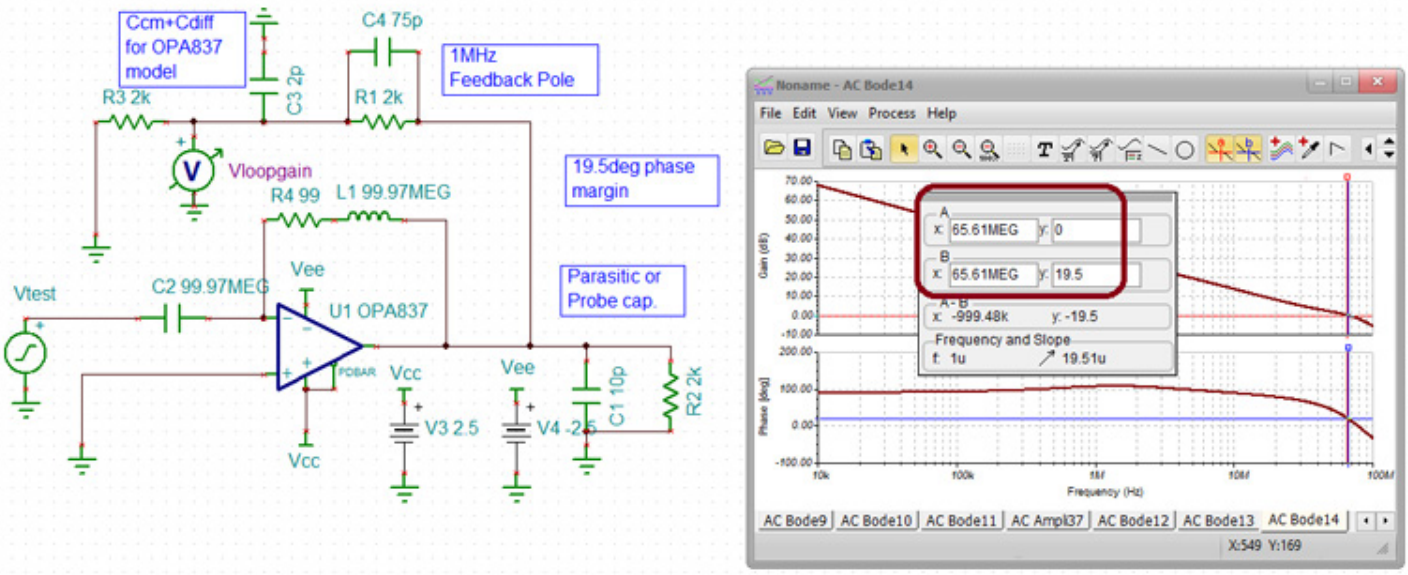
Once we have the I/O ranges satisfied and the output dc error band estimated for particular candidate solution device, the actual functional design can proceed. Many different implementations and applications can call upon the vast range of op amps and FDAs for numerous end applications.

With a schematic and maybe even a layout developed, do you know your phase margin? Perhaps you should. Op amps have always had the risk of instability. It's been exacerbated by the more aggressive designs in recent years trying to deliver the most performance at the lowest power.

For instance, the common RRO stage designs come with a very reactive open-loop output impedance (**Fig. 6**, *"Improved Stability Analysis"*). Hopefully this is in the simulation model. Often, it's a little uncertain if this critical feature to loop phase margin is correctly captured by the model.

A circuit that's already oscillating has one set of bench tools to isolate down to the suspect device. It's for more prudent to attempt a phase-margin simulation prior to board build to head off any problems. That does, of course, depend on good simulation models, and those have been improving. Still, they come with a variety of pitfalls across the industry.

There are several easy techniques to extract the loop phase margin from an amplifier schematic (*"Improved Stability Analysis"*). If possible, any layout and source impedance parasitics should be added to the simulation, and by all means the intended load has to be there—even if it's only a parasitic RC of the next device. Essentially, the simple techniques break the loop in some way, inject a small signal test signal in the loop, and trace the gain and phase around the loop to assess phase margin where the loop gain magnitude goes to 0 dB (or 1 V/V).



7. One possible loop-gain phase margin simulation setup shows only 19.5-degree phase margin for the circuit of Figure 6.

If we think about the transfer function having that LG/(LG+1) term, it can be rewritten as 1/(1+(1/LG)). The LG has a gain and a phase-shift component. If it drops close to a 1 magnitude (0 dB crossover) near where the phase shift is approaching 180 degrees around the loop, it becomes a 1/(1-1) term, which may result in sustained or intermittent oscillation. This can cost lots of manhours and re-spin dollars when a little bit of simulation time could have headed off this pain and suffering.

Even simple circuits can run into phase-margin problems (Fig. 6, again). Here, a simple inverting gain of −1-V/V design added a feedback capacitor to bandlimit the signal channel to 1 MHz. A small parasitic capacitive load, along with that feedback Cf, interacts with the reactive open-loop output impedance to cause the peaking at 74 MHz. This is a warning that the circuit might go unstable in production.

To run a LG phase-margin simulation, it's necessary to first establish a good dc operating point for all nodes in the circuit. Older approaches found the exact input offset voltage to add to an open-loop circuit to zero the output-pin voltage. That works, but it's much easier to use simulation tricks of impossibly high L and C elements to do this job for us, as shown in **Figure 7** using the OPA837 model again.

The large feedback inductor closes the feedback loop at dc, then immediately opens up on the first frequency test step. The large input capacitor is open at dc, then immediately shorts out to apply the test signal on the first frequency step.

This approach requires you to manually add the op-amp input impedance at the loop gain measurement point (2 pF here). The measurement meter is rotated to report phase margin directly for this setup. Looking for the 0-dB gain point around the loop and then the phase margin at that same 66.61-MHz frequency shows only 19.5 degrees. This would require some attention where several approaches (and this phase-margin simulation approach) are detailed in Reference 9.

What your minimum target phase margin might be depends on your circuit and the device you're using. Many older devices (National Semiconductor in particular) targeted a nominal 45 degrees and just took the peaking that results from it. More modern devices feature a nominal phase-margin target around 60 degrees to get close to a Butterworth closed-loop response. As a rough guideline for most circuits:

1. Phase margin >30 degrees is probably okay if the intended circuit operation is acceptable.
2. Phase margin between 20 and 30 degrees, if easy to do, should be improved to >30 degrees.
3. Phase margin <20 degrees probably should be raised to at least the mid 20s.
4. Phase margin <10 degrees—you should never go to production like this; it absolutely needs attention.

How sensitive a design is part to part and over temperature variation really depends on the circuit and devices chosen. Older op amps and FDAs have a wider spread on their open-loop gain and phase where more modern devices (especially those with supply current trim) are much better and will have far lower risk of large dips in phase margin over production.

Keep these three hazardous areas in mind as you set out to apply the vast range of op amps, FDAs, and INAs to your design.

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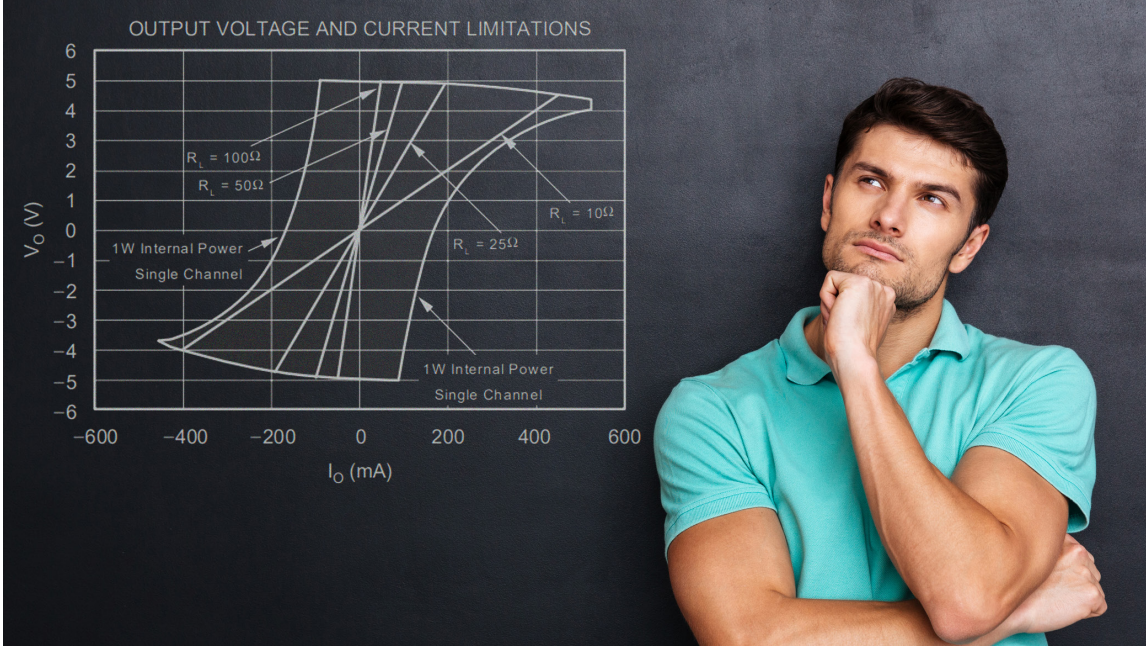


CHAPTER 2:

Why are Specification and Characterizations for Op Amps and FDAs Different and Confusing?

MICHAEL STEFFES, Analog Signal Path Consultant

From input offset voltage to slew rate to gain bandwidth product, specifications for operational amplifiers can vary widely amongst different vendors.

It can be a maddening (and time-consuming) task to compare data across vendors to get a real comparison between possible solutions. Between "marketesse" and just plain deception and/or errors, how can you see through these and normalize critical specs across vendors to get real comparisons.

Having contributed to the development and product launch of over 150 high-speed amplifiers from 1985 forward, the level of detail and tradeoffs going into product datasheets and simulation models probably exceeds the wildest imaginings of the end system designers. Here you will learn some of the hidden background for (and often confusing) specifications along with what to look out for in characterization curves and vendor simulation models.

First, who does this work and what do they bring to the task?

IC design engineer

The designer, working with the latest process design kit (PDK) takes the marketers end-product targets and iterates over many months to get close. Usually, these targets take the form of more and more performance at lower and lower supply current.

Occasionally, a new topology will come along that fills an important niche, such as the fully differential amplifier (FDA) and current feedback amplifier (CFA). Once the nominal transistor-level topology is set, he/she will start running statistical process case and over-temp simulations to extract out corner cases for the proposed end limits on key specs. PDKs have evolved to be remarkably good; only some of that gets into the datasheet and customer simulation models.

Marketing engineer

Looking at the extant solution universe, the marketing engineer tries to carve out unique

and valuable new product targets. Through the course of design and introduction, he/she trades off "don't care" versus "must care" specs with the designer to hopefully emerge with a meaningful new solution for the analog design community.

ATE engineer

This key team member is tasked with layering over a set of probe and/or finished product tests to ensure nothing ships that's defective. In the early days of high-speed amplifiers, 100% ac testing was done at Comlinear Corp on the industry's first current feedback op amps using an HP3577 network analyzer. Over time, it became clear that a full suite of stressful dc tests shipped good ac parts and that production expense was eliminated.

With a few exceptions, all current precision and higher-speed amplifiers receive only a dc test at probe and/or final test at some nominal temperature (with some span on that), imputing ac performance within the designer worst-case simulation results.

The ATE engineer is incentivized to deliver tests and limits with 100% yield. The marketing engineer must resist this—say, on input offset voltage, a ±3.5-sigma test limit is probably adequate (implying no more than 0.04% yield loss). Expanding single-lot ATE data to final datasheet limits is largely internal culture, designer simulation tools, and judgement calls among the development team members and any QA mandates that might be imposed.

Applications engineer

Directed by the marketing engineer, and with an assist from design, the application engineer is tasked with taking the characterization curves and working with the modeling team to develop and test the public simulation model. This is where the rubber meets the road in what the customer sees as a product support package. He/she will also add suitable application text and examples to the final datasheet to illustrate the fabulous new capability for a device that probably cost well over $1M to develop.

Personnel and Datasheet "Churn"

One of the difficulties with consistent and accurate material is the relative turnover in these positions. Often, the designer and ATE engineer are 20-plus-year folks. There's quite a bit of churn in the marketing and applications roles where the latter might be just out of school. Hence, a very tenuous thread links today's datasheets to those done even 10 years ago (and nearly none to those done 20 years ago).

At a more basic level, no NIST reference document exists on how the different specs and characterization curves "must" be done. In fact, on some of the critical specs, there's been an ongoing evolution of better methods.

For instance, when I first started doing distortion plots (circa 1987), about −90 dBc was the measurement limit imposed by spectrum analyzers. Today, bench techniques reach down near −150 dBc (if you want to spend enough effort on it, very non-trivial—operating above audio precision measurement frequency range).

Clarifications on Occasionally Murky DC Specs

Most of the op-amp and FDA dc specifications are pretty clear. Some, but not all, of the dc specifications become the final test lines. A few can cause confusion at times, particularly those with a zero mean as well as the output current specification.

Input offset voltage

The input offset voltage (and current for bipolar inputs) will usually have a distribution centered on zero. Modern devices trim this to a zero mean at either wafer probe or pack-

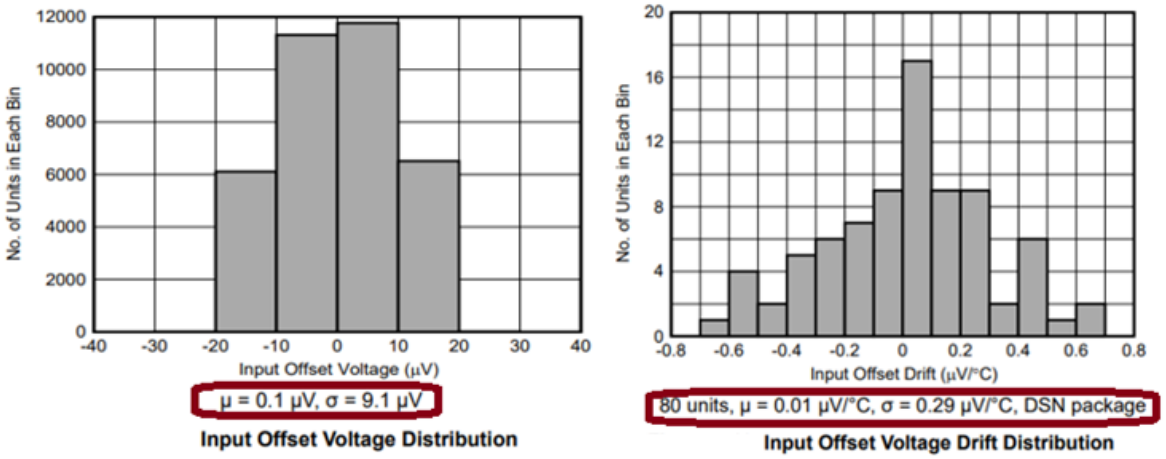
aged eTrim. So what do you specify for a typical, because "0" doesn't really give you much information?

The informal practice across the industry is to report the ±1-sigma number as the typical specification to avoid customer surprises when devices with a zero mean don't test at zero for typical devices. Specifications for a maximum input offset voltage (and current where needed) are extremely inconsistent. Essentially those are a combination of a plus/minus shift of the mean off of zero plus/minus some number of standard deviations.

My practice was to impose a ±3.5-sigma range (THS4551) to accept approximately 0.04% yield loss. Other devices and product groups allow for much wider limits (OPA837, THP210, ADA4805, etc). Some of this is related to test repeatability, where there's also an error band in test over different physical testers. While this might pass more units, you do wonder if devices way out on the distribution tails (some allow for >8 sigma) might be shipping "defective" units.

These same issues apply to the specified input-offset-voltage temperature drift, where it's extremely rare to see this as a 100% tested specification (the JFET input OPA656 is one of the very few). Maximum offset drift numbers are sometimes provided without ATE screens (OPA2683A, ADA4895), while many more devices have no maximum drift spec(s).

The guaranteed maximum drift numbers are from extensive bench characterization of packaged units that are (hopefully?) at the extreme allowed limits of the tested room-temp input offset voltage (and current where appropriate). Drift magnitude is often linearly related to initial offset, so testing units at the allowed limit should expose the worst-case drift specs.



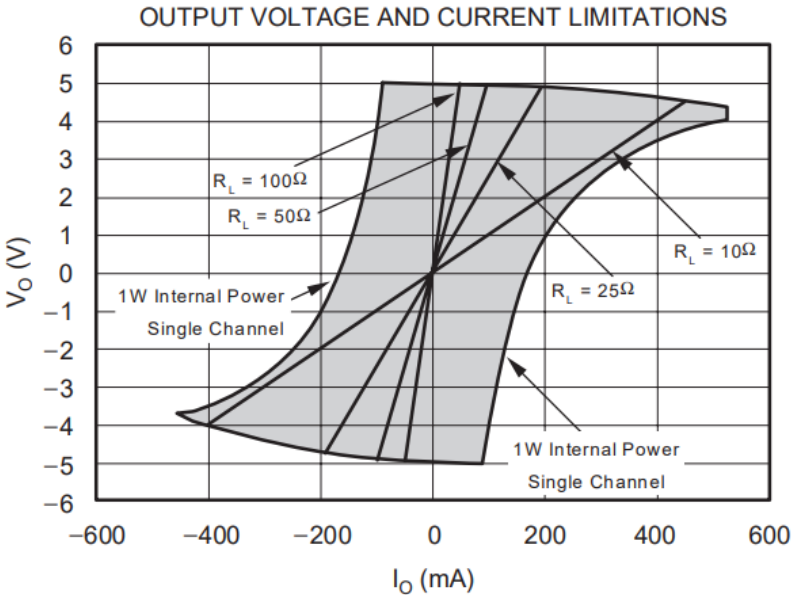
1. Recent OPA2863A offset and offset drift histogram examples show widely different plus/minus sigma limits.

Figure 1 shows a recent example where the tested Vos limits are ±95 µV (or ±10 sigma), imputing a drift limit of ±1.2 µV/°C or ±4 sigma. The actual Vos histogram data in Figure 1 is much tighter than the ATE limit in the specification table. Apparently, the ATE engineer got this through while the marketer was out traveling.

Output current

Probably the most slippery dc specification on any op-amp or FDA datasheet is the output current. Marketers want the biggest number possible. Designers struggle with that as large output devices bring an increased capacitance, which adds open-loop phase shift that impairs achievable bandwidth on ever-declining supply current budgets. ATE engineers are all over the map in how this might be tested.

Physically, the output-current demand will get involved with the available "linear" out-

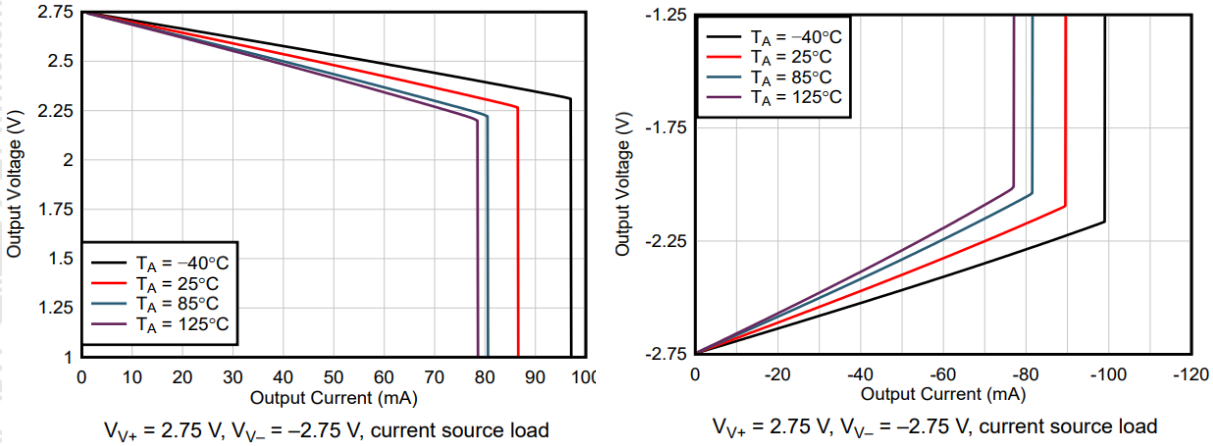


2. Shown is an example four-quadrant output VI limit for a dual CFA high power PLC line driver.

put-voltage swing available. Every device (even rail-to-rail outputs) will see an increase in required headroom to the supplies for linear operation due to rising load-current demand. Keep in mind that not only the actual load, but also the feedback network, is part of that load. In non-inverting configurations, that's the sum of the feedback and gain resistors, while in inverting configurations (and for FDAs), it's just the feedback resistor appearing in parallel with the actual load.

First, it's important to recognize that any "short circuit" current specification is usually a self-limited (base or gate drive) typical specification. Traditionally, it needs to be there, but it doesn't really give you much information. Only when there is a min. or max. specification is there an "active" current limit in the output stage design (THS3491), with some exceptions (OPA2683A).

Over time, several different efforts at a "linear" output-current specification have been attempted. During the PLC line-driver developments (where the line can push current back into an amplifier output), a foour-quadrant envelope of limits was shown – like that in **Figure 2** taken from the OPA2674 datasheet (on ±6-V supplies). Only the quadrants with the load lines describe normal operation here.



3. Compared are the output swing vs. current for the RRIO precision OPA328.

Maximum current into a resistive load	$T_A \approx 25°C$, ±1.6 V into 27 Ω, $V_{IO} < 2$ mV	±58	±70	mA	A
Linear current into a resistive load	$T_A \approx 25°C$, ±1.7 V into 37.4 Ω, $A_{OL} > 80$ dB	±45	±50	mA	A

4. This is an example linearity test for output current and voltage into a resistive load for the OPA837.

More typically, a bipolar "claw" curve has evolved to describe the loss of output headroom, as more sourcing or sinking current is required. Here, the two polarities are separated into two plots, but the increase in required headroom with output source/sink current is clearly shown in **Figure 3**.

These output limits are hard limits (usually from simulation). However in final ATE, a more common test is a minimum AoI test at some conservatively guardbanded (25°C) test point. It exercises most of the available output current (from worst-case designer simulations at 25°C) at the maximum swing to rail available at that current draw, as shown in **Figure 4** for the OPA837.

Here, the final ATE test lines are clearly designated by the "A" test level, and the test conditions to produce these stated output currents are shown (using ±2.5-V supplies in this case). This type of ATE screen is intended to ensure that no "weak" output stage devices are getting into inventory.

These issues apply to all op amps and FDAs. It is, however, often not clearly shown in the customer support material and almost never accurately modeled in the vendor simulation models.

Common Hazards in Interpreting Op-Amp and FDA AC Specs

If the dc specifications have some typical traps, the ac specifications are often much worse. Again, none of these are tested on an outgoing basis and the typical—and much more rarely guaranteed—ac specifications (e.g., OPA2677) come completely from simulation. Usually, a single (hopefully typical) lot of early material is characterized one time at product release.

Vendor models are normally bounced against typical designer simulation with some first-lot material validation. A few very typical performance parameters are prone to error and/or confusion.

Input spot noise

The input spot noise voltage must be in every datasheet. Physically, these always have a 1/f corner that varies considerably more than the higher-frequency "flatband" number (except for chopper-input VFAs, which have a flat noise spectrum down to dc but then add noise spurs at the higher chopper frequency).

A very old convention for relatively slow (often precision) amplifiers is to report an input spot noise at 1 kHz. This apparently came out of the audio world and the 1-kHz number may be above, or below, the 1/f corner. It's much more descriptive to specify a typical flatband number (most higher speed amplifiers do this) above the 1/f frequency and then a typical 1/f corner.

However, many VFAs quote a single noise number and only after some digging can you discern if that's the 1-kHz number. You must then consult the swept-frequency input spot noise plot to decide what that means.

Gain bandwidth product

The second most confusing ac specification has become the typical gain bandwidth product (GBP) for VFA op amps and FDAs. Classic theory describes this as the 1-pole projection

to 0-dB crossover for the devices' AoI curve. Modern devices have higher-frequency open-loop poles (and sometimes pole/zero pairs, LT6363) in the AoI response that convolutes this quite a bit.

Since the new product characterization folks are a revolving door of new grads, many datasheets erroneously report the GBP as the AoI = 0 dB frequency.[1] That's never very close for decompensated devices and often even a bit off for unity-gain stable devices. This confuses new grads quite a bit since the closed-loop small-signal BW (SSBW) never really was accurately described by the GBP idea even for unity-gain stable VFAs.1 Lower phase margins at loop-gain (LG) crossover always extend the closed-loop SSBW far beyond the GBP model (below 65-deg. phase margin, which is approximately a 1.6X extension).

Sometimes, those new grads try to force a fit to the simple GBP model by modifying what they report. It's always best to confirm the single-pole GBP in simulation for design work (go to the 40-dB AoI gain frequency and multiply that by 100X to get the single pole GBP, **Figure 6** shows a simulation setup). Oftentimes, that's far different than what shows up in the datasheet, and hopefully the modeling effort worked closely with the designer to emulate the new devices' typical AoI gain and phase-match the designer PDK simulations.

Slew rate

Slew rate has long been a difficult specification and fraught with error. Early ±15-V op amps showed a very distinctive, limited dv/dt on a large output transition. Sometimes those are different for rising and falling, where reporting the faster rate in the specification table is not uncommon. With few exceptions, a signal that rises with a certain maximum rate must also fall at a similar rate. Check the plots to see if this bit of chicanery is at play (Figure 39 in the OPA192 datasheet).

In most applications, the available slew rate is like a hard output transition rate that should be avoided, if possible, in application. By definition, the feedback loop has opened up if the output is slew limiting where that recovery time to a closed-loop final condition is rarely specified—and if so, only for limited number of external operating conditions.

The best way to explore edge transition rates is to plot the measured or simulated point by point dv/dt on the edges.[2] This will clearly show when an edge has hit a slew limit (flat dv/dt) and more detail is going into and out of slew limiting.

Harmonic distortion

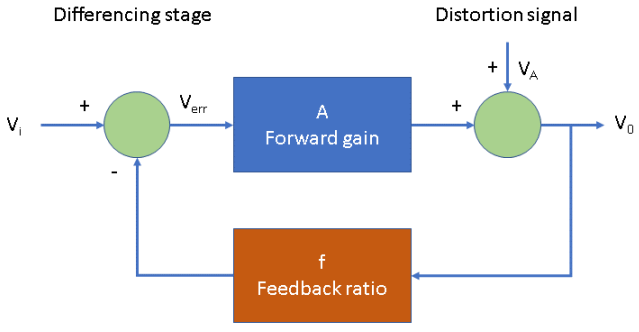
One of the more difficult characterization requirements in any new op-amp or FDA development is a range of typical harmonic-distortion plots. These have evolved over the years to show performance to ≤145 dBc on occasion. The main reporting difficulty is all of the different conditions that influence the measured values, including:

$$\begin{cases} V_0 = A * V_{err} + V_d \\ V_{err} = V_i - f * V_0 \end{cases}$$

$$V_0 = A * V_i - A * f * V_0 + V_d$$

$$(1 + A * f) * V_0 = A * V_i + V_d$$

$$V_0 = A * \frac{V_i}{(1 + A * f)} + \frac{V_d}{(1 + A * f)}$$



5. Fundamental harmonic distortion correction in negative feedback op amps or FDAs.

- Supply voltages
- Gain (more precisely, the loop gain over the testing frequency span)
- Output loading (and this includes the required feedback network)
- Output voltage swing

Frequency of the test fundamental (or two of these for two-tone intermodulation testing)

This myriad of test conditions does make it relatively difficult to compare data across different possible solutions. It's important to always keep in mind some fundamental harmonic-distortion facts. Essentially, the output closed-loop distortion terms are the open-loop distortion terms in the output stage corrected by the LG at the fundamental frequency of testing. The LG is A*f* in **Figure 5**.

The easiest way to show a better HD number in characterization is to test with a lighter resistive load. Be careful comparing devices on their stated loading under test.

Hidden Traps in Vendor-Supplied Simulation Models

As a new op amp and/or FDA approaches public release, the modeling effort gets underway. Over time, several approaches have dominated:

- *Simplified full transistor level models:* These can be very good if the embedded transistor models capture enough of the available parameters (Comlinear models, full netlists are in the TINA libraries showing detailed transistor models).[3] Some transistor-based models use such a simplified core transistor model that they're nearly useless.
- *Boyle model:* This is more of a behavioral model that does okay on basic things, but often isn't very accurate.[4]
- Custom block diagram types of models that can capture quite a lot of the device characteristics:[5] In this case, the internals are often company confidential and sometimes those models are encrypted.

How this is organized inside a company makes a huge difference in the effectiveness of these models. Some groups have each project's individual application engineer and/or designer do these (which leads to lots of modeling variations). Some have a dedicated modeling group that usually leads to throughput bottlenecks. Others have a designated applications specialist in each development group that becomes the resident expert. This will yield better and better models with some consistency, until they move on to another job.

One theme here is that the op-amp and FDA models have been getting regular updates from some of the vendors. Designers should certainly try to verify that they're using the most recent update, as earlier (more error-prone) models are still available from some legacy sources.

Importantly, the vendor models must assign some typical dc value specifications where their "range" is never captured. Therefore, dc parameters are just enough—they don't span the full range of the datasheet specification limits. Far more effort is put into the ac performance characteristics, but again, only typical. To get a good prediction of small-signal ac performance over a wide range of external application circuits, the model must have very good:

- Open-loop gain and phase modeling.
- Open-loop output impedance modeling (this has become relatively involved with RRout devices).

- Accurate input impedance modeling. This is usually mainly input capacitance, but for CFA devices a good inverting-input impedance model is necessary (usually just a low R value; however, for instance, the THS3217 OPS model includes a series RL into the inverting input and parasitic C to ground on that device pin).

An op amp's open-loop gain or phase is really the core value proposition for the ac aspect of the device. There are numerous approaches to extracting this from the vendor model. **Figure 6** shows one simple approach.

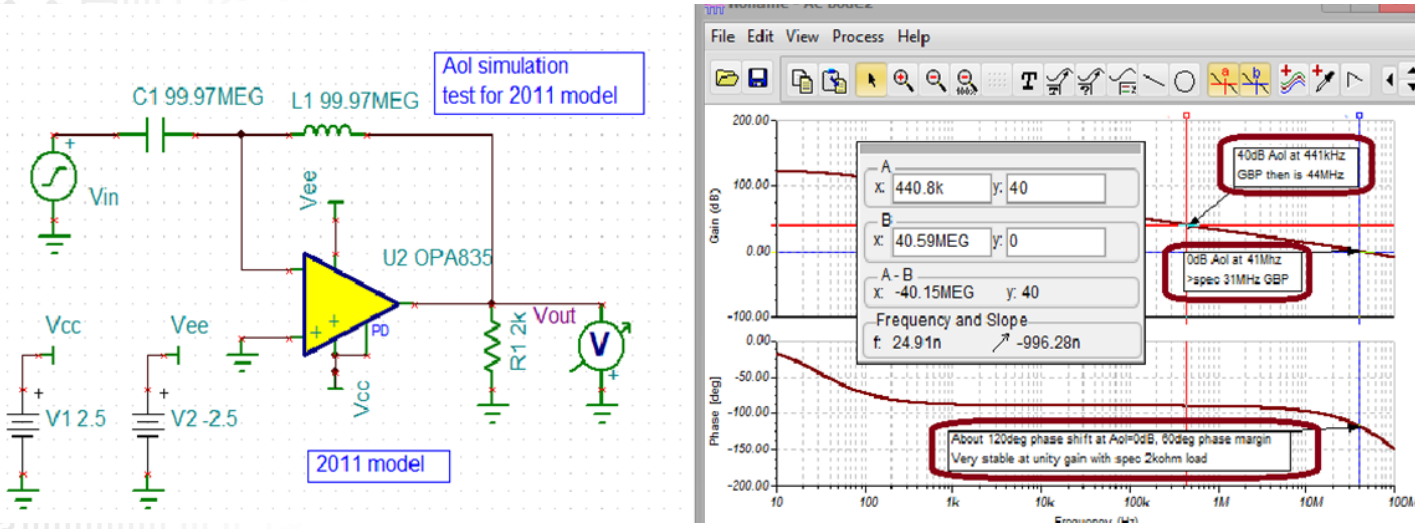
Typically, these are done with split bipolar supplies with the V+ input grounded and the test signal injected into the inverting input. It's critical to load the amplifier with the stated resistive (and/or capacitive) loads noted in the datasheet.

This approach applies a simulation trick to close the loop at dc at unity gain using a ludicrously high feedback L value, and then injects the small-signal ac test input through an equally high input capacitor. These elements set up a midscale dc operating point and then disappear on the first ac frequency step. Since the input is into the inverting input, the output meter here is rotated 180 deg. to report Aol, where its phase starts out at 0 deg. and proceeds toward −180 deg.

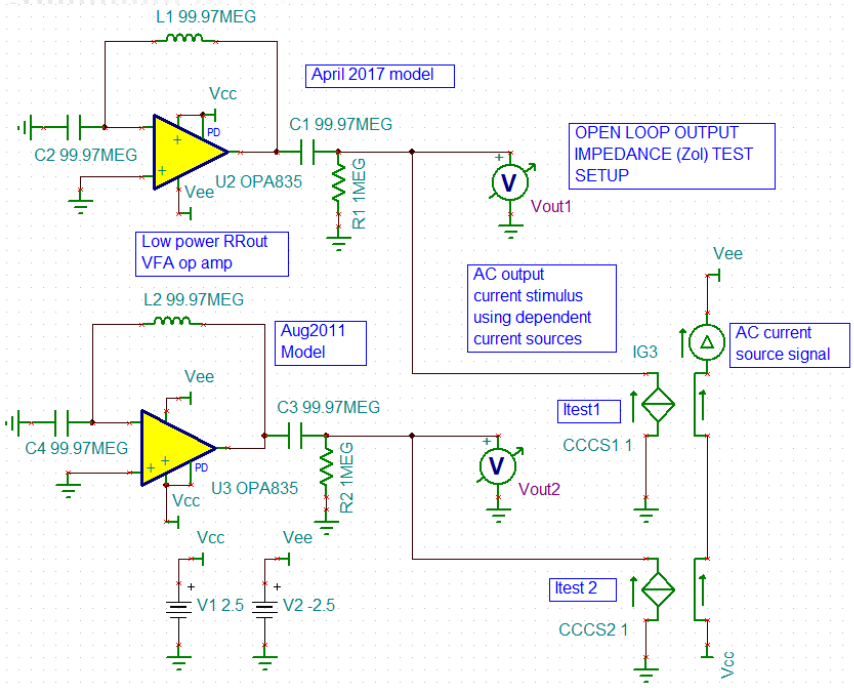
This model shows quite a bit more GBP than the specified typical of 31 MHz. The 0-dB crossover is less than the predicted single-pole GBP due to the higher-frequency Aol poles indicated by the phase shift moving down −90 deg. from the single pole. This OPA835 model is now updated to a 2017 revision, where this simulation shows a correct 31-MHz GBP projecting from a 40-dB Aol point.

One of the modeling oversights receiving much attention in recent years is the open-loop output impedance. Early bipolar op amps and FDAs offered a very power-efficient Class AB output stage that delivered lots of current with a low dc open-loop output resistance going inductive at higher frequencies.

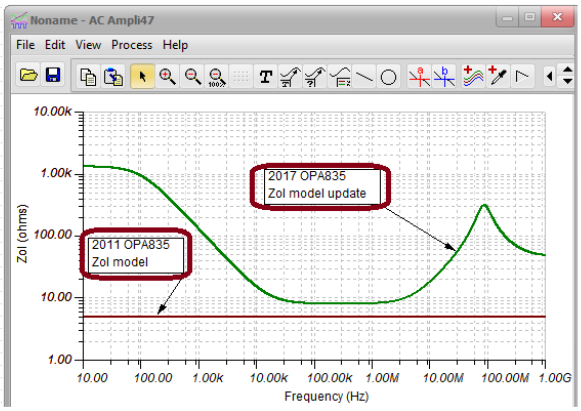
Those required considerable headroom for the supplies, where more recent devices have gone to RRout structures. The output stages show a considerably more involved open-loop output impedance6 that was completely missed in much of the original modeling. They're getting updated over time as shown in the OPA835 Zol simulation of **Figure 7**, going from



6. This is an example of Aol gain and phase simulation using the OPA835 2011 model.



7. Open-loop output impedance simulations were performed for the OPA835 RRout low-power op amp.



the 2011 to 2017 model updates. The high-frequency resonance in the RRout Zol can sometimes lead to closed-loop peaking or oscillations with relatively simple external conditions.[7]

The last key issue for accurate ac modeling involves the input impedances. For VFA op amps, these are usually just the common-mode and differential-mode input capacitances. Usually, these relatively low value elements will not interact with lower-speed (<10 MHz) device applications, but they become critically important for higher-speed op amps and FDAs.

Once again, some of the legacy models have these in the model incorrectly, where that's being repaired over time. At minimum, when using a higher-speed device in simulation, confirm that the model values match the datasheet values (from designer sims) using the approaches detailed in Reference 8.

As you endeavor to select and apply modern op-amp and FDA devices, keep in mind some of these inconsistencies across vendors and modeling pitfalls that pervade the industry. Working through these can be difficult, but when armed with what to look out for, supplier application teams can be a great help.

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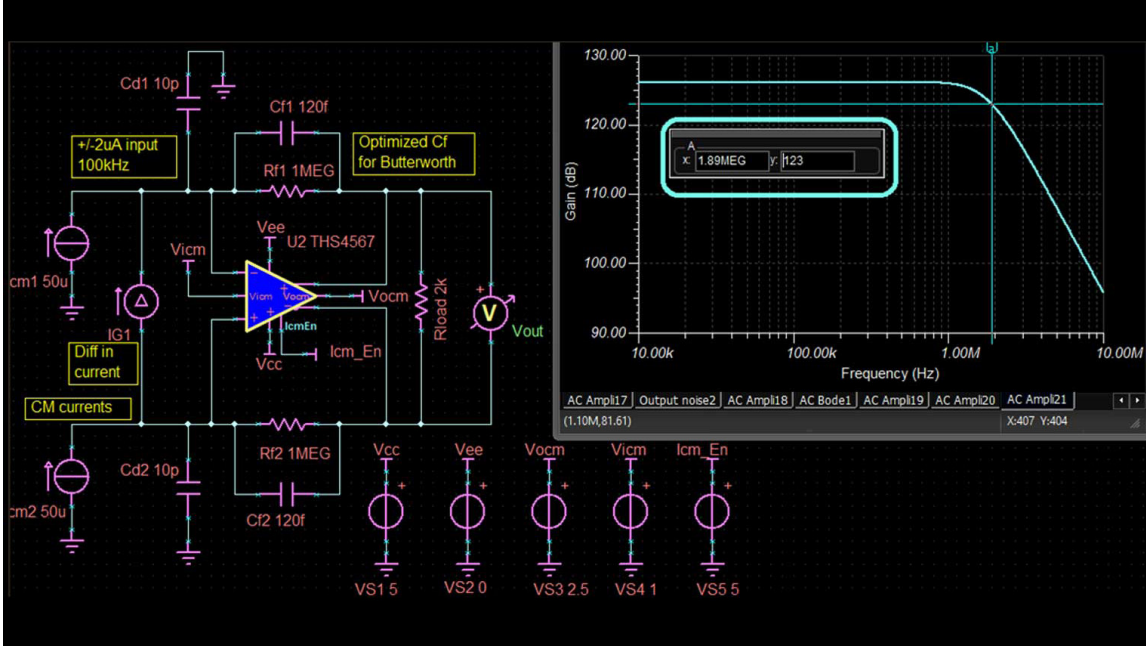


CHAPTER 3:

What Signal-Path Developments are Still Missing from Textbooks?

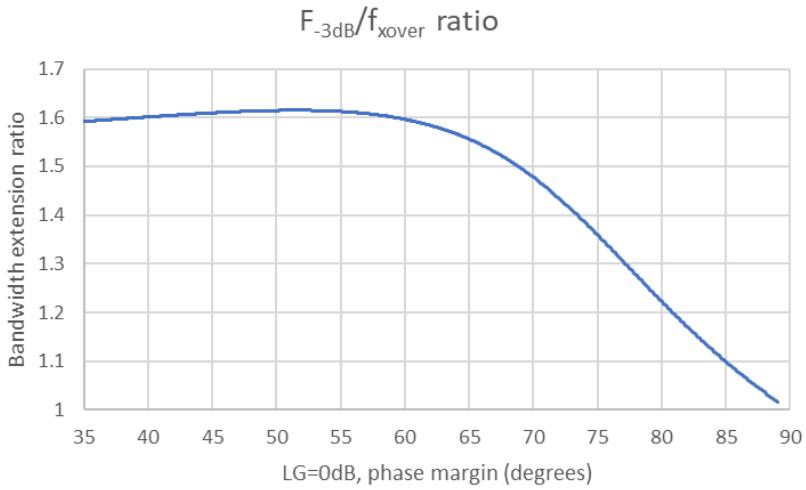
MICHAEL STEFFES, Analog Signal Path Consultant

Here's what you didn't learn in school, such as how to really combine the distortion terms in cascaded amplifiers.

Industry amplifier development groups continue to improve on devices and analysis techniques, publishing those in datasheets, application notes, industry articles, etc. But these rarely find their way into textbook updates. Read on for a representative sample of what you might have missed in your EE education.

The classic gain bandwidth product (GBP) idea was always an oversimplification. One simple plot yields much closer SSBW versus gain prediction for any voltage feedback amplifier (VFA) or fully differential amplifier (FDA).

The well-known GBP model predicts that the closed-loop small-signal bandwidth (SSBW) will simply be the GBP divided by the noise gain (NG). The NG is the inverse of the voltage divider from the output pin back to the feedback input pin(s). In a non-inverting VFA design,



1. The SSBW extension over the LG = 0 dB (fxover) phase margin.

the NG will be the same as the desired signal gain.

It doesn't take very long in characterizing SSBW over gain for VFA amplifiers to find out that this model is not very close at lower gains. The model is assuming a single-pole loop gain (LG) condition, where that's hardly ever the physical case. A second-order model gets much closer, but it too is still an approximation for most modern VFA op amps and/or FDAs.

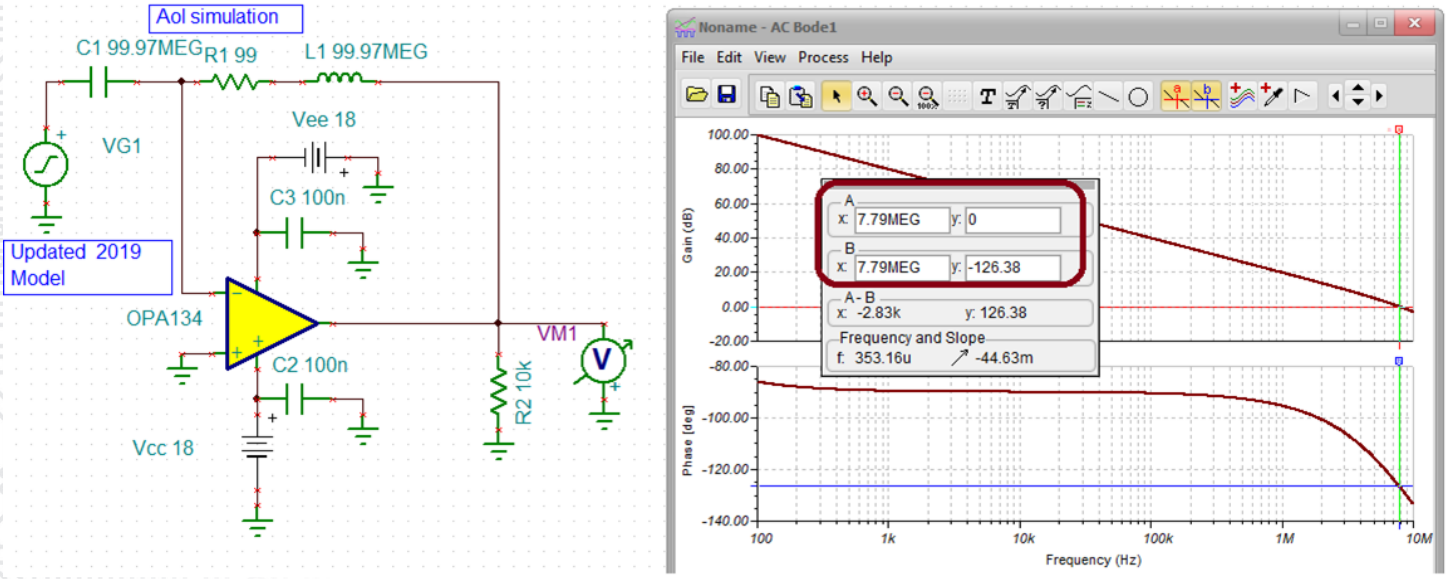
Almost any modern (but accurate) VFA model can be used to illustrate these effects—even allegedly unity-gain stable devices. All IC designers (and most marketers) know that designing a unity-gain VFA op amp for about 65-deg. phase margin will give far higher closed-loop SSBW than the GBP might predict (≈1.55X). A nominal unity-gain, 65-deg. phase-margin design is very common, yielding an approximate closed-loop Butterworth design (at least second order by definition).

The approach to generate **Figure 1** was to introduce a NG zero to a single pole Aol analysis by adding a tuning capacitor at the inverting node to ground for an inverting op-amp configuration. Solving for the loop gain (LG) = 0-dB point, as that zero is reduced in frequency (ramping that capacitor up), will yield one quadratic.

Then, at that same capacitor value, the LG phase margin is used to solve for the closed-loop second-order Q, and subsequently the resulting F-3dB. The ratio of that F-3dB to the LG = 0-dB frequency is formed to get Figure 1. Note that for phase margin < 65 deg., the closed-loop response will also be peaking.[1]

A good example can be shown using the OPA134 simulation model. **Figure 2** shows the Aol gain and phase simulation,1 which would be the same thing as the LG plot for a unity-gain configuration.

This simulation shows 54-deg. phase margin, which, from Figure 1, should give a close-loop gain of 1 SSBW extension to 7.79 MHz*1.61 = 12.54 MHz. The gain of 1 simulation in **Figure 3** shows a 13.6-MHz F-3dB with 1.8 dB peaking. Ideally, a 54-deg. phase margin should be giving about 1.2 dB peaking (Fig. 2)1, so these results are close, but not exact, to the expected response shape due to higher-order poles in the model not captured by this second-order analysis.



2. Open-loop gain and phase simulation for the OPA134 VFA op-amp model.

The curve of Figure 1 adds a lot to our understanding of the closed-loop SSBW over gain versus the simple GBP model that would have predicted only 7.8-MHz F-3dB unity-gain bandwidth.

How do you really combine the distortion terms in cascaded amplifiers or amplifier + ADC systems? Legacy power summing calculations are quite incorrect.

One of the fundamental questions in an analog-to-digital converter (ADC) driver application is how low do the harmonic-distortion (HD) terms need to be coming into the ADC to only slightly impair its performance. Numerous early efforts at this simply added powers as if the individual distortion terms were in a 45-deg. (quadrature) relationship.

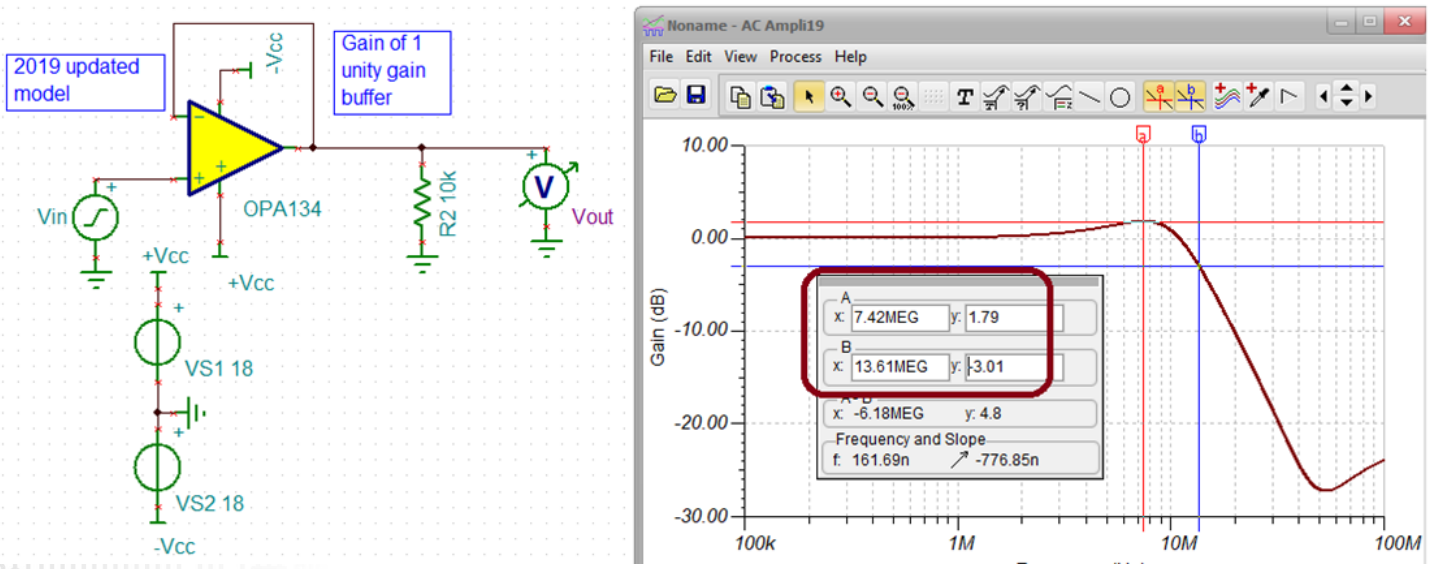
In fact, the individual input distortion terms must be added linearly to those same terms for the ADC itself. Extensive testing with individual FDAs (THS4509) and high-speed ADCs (ADS5500), where each device was separately characterized then combined, proved that the individual distortion terms add in phase as voltage vectors.2 The math combining two cascaded stages for each distortion term is shown as Eq. 1:

$$SFDR_{System} = -20 \cdot log\left(10^{\frac{-SFDR_{ADC}}{20}} + 10^{\frac{-SFDR_{Amp}}{20}}\right) \qquad (1)$$

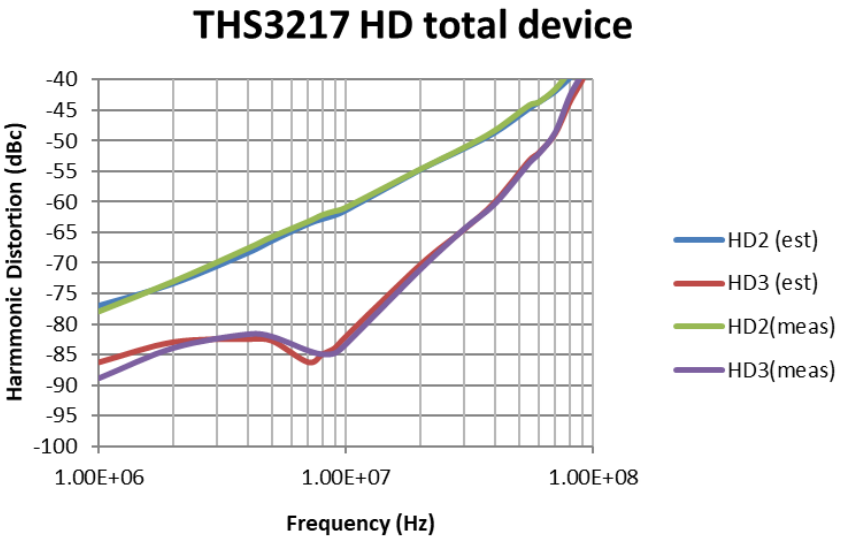
This is written as spurious-free dynamic range (SFDR), but actually the HD2 and HD3 (etc.) terms would be combined individually. Legacy literature would often report the combination as a total harmonic distortion (THD) power combination as in Eq. 2, which is totally incorrect, (page 43, ref. 3):

$$THD_{system} = \sqrt{THD^2_{Amplifier} + THD^2_{ADC}} \qquad (2)$$

Much more recent bench testing of a two-stage amplifier (THS3217), where the input and output stages were measured separately, then combined in cascaded stages, showed these same results (**Fig. 4**). Here, the input D2S stage was tested over frequency with a 2 V p-p



3. Gain of 1 OPA134 simulation showing 13.6-MHz F-3dB and 1.8 dB peaking.



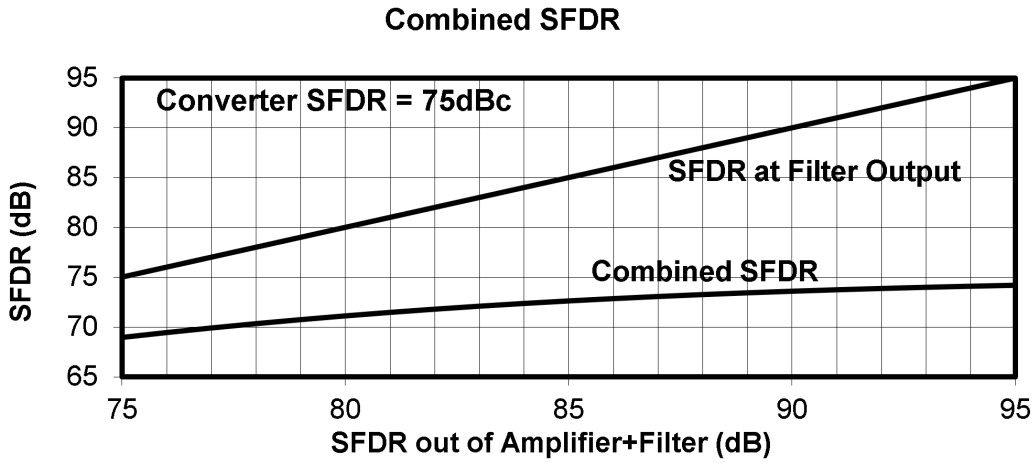
4. Calculated and measured two-stage amplifier distortion comparison.

into 200-Ω load, while the OPS stage in that same unit was tested separately producing 5 V p-p into 100-Ω load.

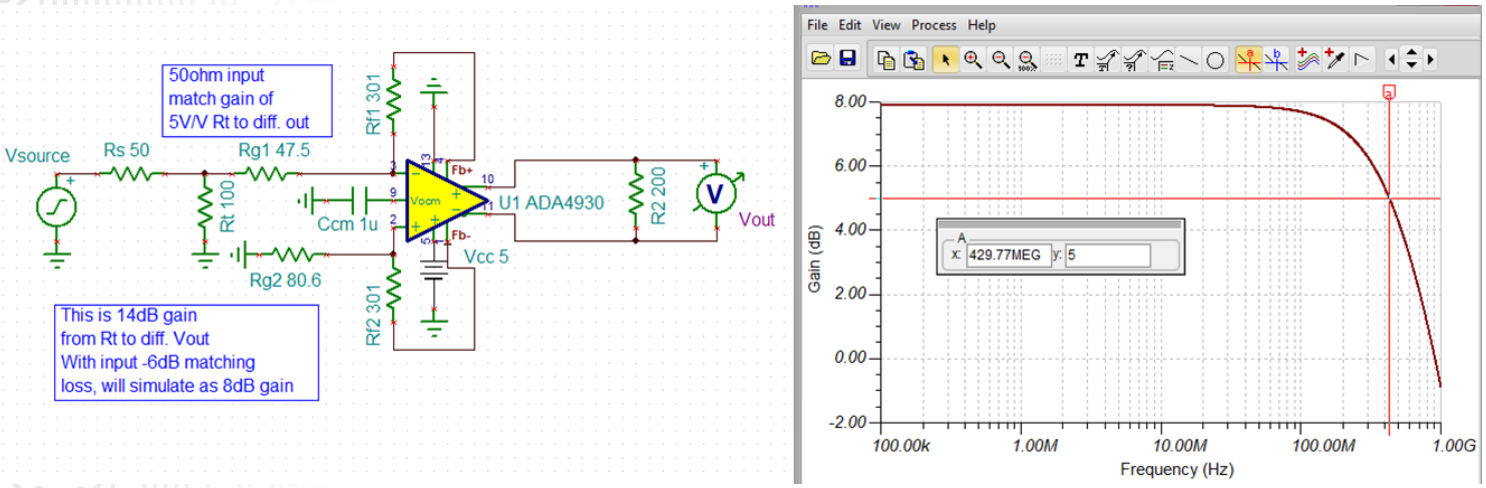
These separate measurements were combined using Eq. 1 to predict the cascaded distortion. Then the same part was measured in a cascaded configuration producing the same swings and loading at each stage. Clearly, Eq. 1 appears to correctly combine the cascaded distortion performance.

Imagine coming into an ADC (or second amplifier stage) with a large fundamental carrier that has its own HD2, HD3, etc., harmonic distortion terms. The ADC (or second amplifier stage) will generate its own harmonic terms from the large fundamental and combine those "in phase" with the terms coming into its input. This makes the problem of minimal ADC degradation much more difficult than predicted by the legacy (and incorrect) power addition assumption of Eq. 2.

Sweeping Eq. 1 for a fixed ADC SFDR term and an improving input-signal SFDR term shows a slowly closing gap in **Figure 5.** For any ADC spurious term reported, degrading it by less than 1 dBc requires an input term at least 20 dB lower than the ADC reported number. This example was for a −75-dBc ADC spur, but it generally holds for any starting level.



5. Combining spurious at the ADC input and the ADC spurious into a final result.



6. Single-to-differential dc-coupled gain of 5 V/V with a 50-Ω input match using the ADA4930 FDA.

The fully differential amplifier (FDA) combines a differential + common-mode (CM) control loop. Hiding inside some FDAs is a very low noise active balun capability.

The first FDA—the AD8138—emerged in 1999. It was an ideal solution for converting single-ended signal paths to the differential drive required by the high-speed pipeline ADCs that had started to emerge in the mid-90s. As FDA bandwidths increased (far beyond 4 GHz today), the need for a matched input impedance was obvious.

However, the FDA's two-loop nature rendered the solution for the required resistors to provide that single-ended impedance match, as well as the desired differential gain, very elusive. In fact, both National Semiconductor and Analog Devices capitulated on that analysis4 and developed solutions that were in fact iterative to simultaneously match to some source impedance and deliver the desired gain.

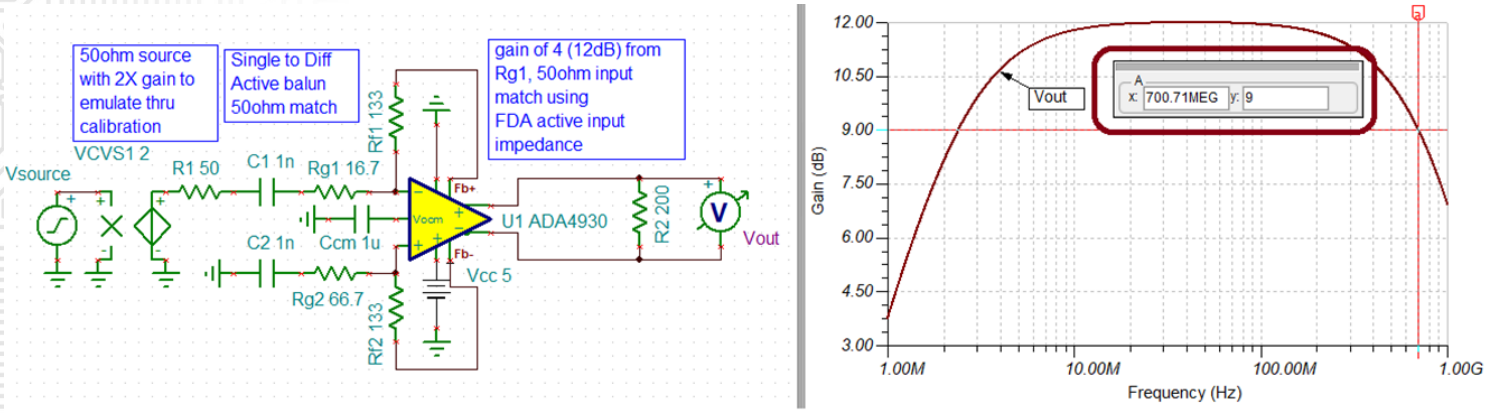
Sinking deep into an algebraic morass in the 2012 timeframe, I extracted a closed form solution for the input resistor to ground (Rt) as Eq. 3:

$$R_t^2 - R_t \frac{2R_S\left(2R_f + \frac{R_s}{2}A_v^2\right)}{2R_f(2 + A_v) - R_sA_v(4 + A_v)} - \frac{2R_fR_s^2A_v}{2R_f(2 + A_v) - R_sA_v(4 + A_v)} = 0 \qquad (3)$$

Figure 6 shows an example gain of 5-V/V design, first picking Rf = 301 Ω, then solving for Rt and subsequently the two Rg values to give a 50-Ω input match. The FDA CM loop will move the CM input voltages with the input signal to generate the output voltage on the non-signal input side. This has the effect of making the apparent impedance looking into Rg1 higher than the physical value (*100-Ω active impedance in* ***Figure 6***).

With Rt solved, the series input gain resistor is then resolved for a selected Rf value.[4] While Eq. 3 looks too complicated to be either correct or useful, it's in fact both. In the original work, I tested these results against both the ADI and NSM tools, delivering identical results for the required R values. Starting with a selected feedback Rf value is required to apply current-feedback-based FDAs.

So, what does this equation offer over the equally effective iterative approaches? Recalling that this equation is for the (kind of extra) resistor to ground (Rt) at the input to attain an impedance match, what if we solved the denominator expression for a zero value? That



7. Active balun single-resistor match to 50 Ω and a gain of 4V /V to the differential V_{out}.

will eliminate this extra Rt resistor to ground, leading to the lowest noise ac- or dc-coupled matched input impedance single-to-differential FDA interface.

Unlike typical magnetic baluns, commonly used in higher-frequency RF channels, this solution can be truly dc-coupled. This "active balun" solution offers a new signal-path processing option for single-to-differential requirements up to an ADC.[5]

While the ISL55210 would be the lowest-noise (0.85nV/√Hz) device to apply here, **Figure 7** shows an example design using the 1.4-nV/√Hz noise ADA4930. Here, the 2.4-MHz, lower F-3dB is set by the 1-nF blocking caps and could be lowered using higher capacitor values.

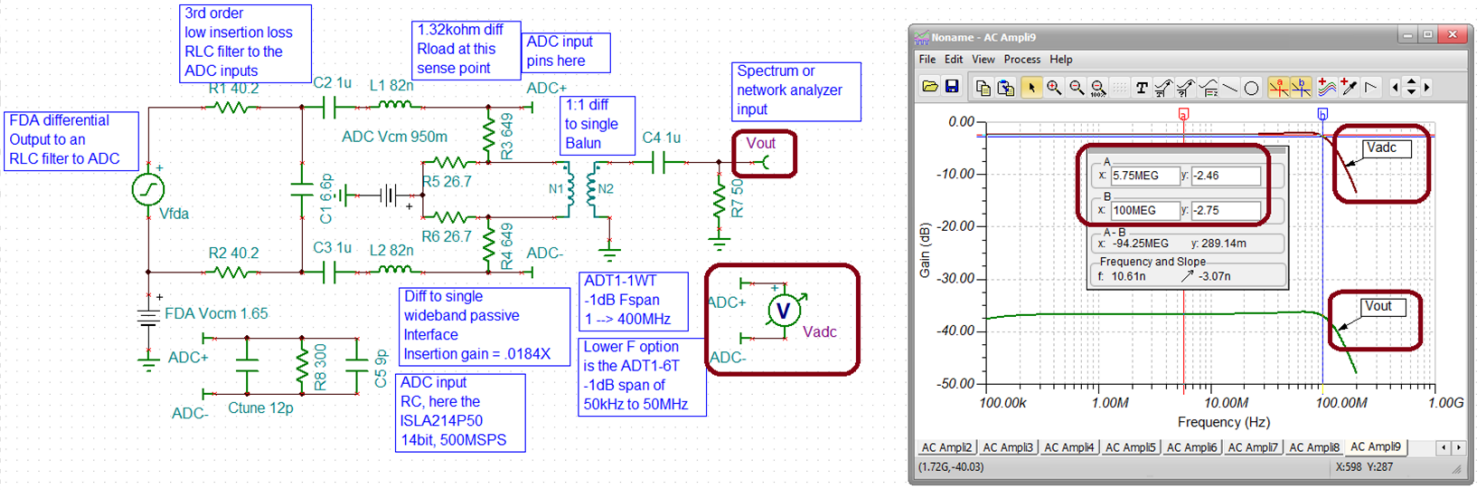
This 12-dB gain stage (from Rg1) gives about 200-MHz flat span with 700-MHz F-3dB. That Rg1 = 16.7 Ω is in fact providing a 50-Ω input match using the active impedance feature of a single-to-differential FDA stage.5 For this to work broadband, the internal CM loop bandwidth must be on the order of the differential loop—they are for these higher-speed FDAs. That CM loop bandwidth is much higher than the reported bandwidth from the control pin to the output CM voltages.

Running an output differential spot-noise simulation shows only 4.2nV/√Hz; the input refers to about 1 nV for this gain of the 4-V/V stage. The input referred noise here is actually less than the specified 1.4-nV FDA input voltage noise, since the signal gain of 4V/V is slightly more than the noise gain of 3 V/V. This 1-nV input spot noise translates into 7.8-dB noise figure for a 50-Ω source and Ta = 17°C.

How would you really interface from an FDA to an ADC while also implementing a direct response shape or harmonic distortion measurement with the ADC input pins down to −110-dBc levels?

The significant effort devoted to delivering a very-low-distortion input signal to an ADC, with some desired frequency-response shape, then combines with the ADC distortion and frequency response terms. Differential probes can be used at the ADC inputs to verify the response shape or step response, but they don't have the dynamic range to extract out the distortion performance for the best interfaces.

Starting from a simple RLC interstage filter[7] design (adapted to differential for an FDA-to-ADC design), that last parallel resistor across the ADC inputs can be split into a very high-dynamic-range differential to single-ended test port to measure the response shape and harmonic distortion right at the ADC inputs.



8. Example RLC filter interface with wideband passive output sense path.

These ideas show up in a fully developed and tested evaluation (EVM) boards using a 4-GHz low-noise FDA (ISL55210) with a 14-bit, 500-MSPS ADC.[8] The aim was to provide a flat 100-kHz to 100-MHz gain of 15-dB interface with minimal signal-to-noise ratio (SNR) and SFDR degradation over the ADC-only specs. That was achieved indicating the SFDR at the ADC inputs was ≤110 dBc through 100 MHz driving 1.8 V p-p differentially at those ADC input pins.

The RLC filter design was necessarily a bit iterative as both the board parasitics and ADC input C were somewhat uncertain. The RLC filter design intentionally targeted a final differential C at about 2X the ADC reported internal value to enable some range for tuning the final external C value down.

That proved trivial as the exact response shape to the ADC inputs (while sampling) was available through the interface described here. Board-level tuning on that last C reduced it to only 1 pF. This signal sense technique can be applied right at the input of any ADC interstage filter design with good results. It's necessarily ac-coupled but suitable for the intended network- or spectrum-analyzer measurements.

While the starting point for this RLC filter design is second order,[7] the design went third order with that added differential C right after those first resistors (**Fig. 8**).

Going left to right in Figure 8:

- The FDA differential outputs drive the filter with an output common-mode dc voltage that optimizes the SFDR out of the chosen FDA (1.65 V here, for example)
- Those first small 40.2-Ω resistors isolate the FDA outputs from the reactive loading of the LC elements. They will also introduce a small insertion loss in the filter to the final differential Rload (−2.45 dB here).
- To isolate common-mode voltage setups from the FDA to the ADC, series 1-µF blocking caps are inserted in the signal path. This is okay for the measurements here, but the interface could also be dc-coupled to the ADC input pins with a bit more effort.
- The differential C, series L's and total final differential C form the third-order filter. This ADC specified a 300 Ω||9 pF differential input Z where an external tuning Ctune is added to fine-tune the filter flatness in this simulation (it also is used to fine-tune the measured response flatness in the final EVM[8]).
- The filter design called for a final single-ended R of 122 Ω. With half of the ADC's internal

300 Ω forming part of that, the external single-sided R's needed to be 662 Ω. The sense path interface passes through a differential-to-single-ended balun conversion (here using the Mini-Circuits ADT1-1WT) to a final 50-Ω measurement instrument termination. That reflects back to the input side of the balun as 25 Ω on each side in parallel with the physical 26.7 Ω. Those combine to 12.9 Ω to form a total of 12.9 Ω + 649 Ω = 662 Ω as required for the filter design.

- The actual design flow for those two resistors targets a total input resistance, including the reflected 25 Ω from the test instrument, and sets a source impedance (26.7 Ω||649 Ω) looking back from the balun primary matching that's 25 Ω for each side on the balun inputs (50 Ω total).
- Since blocking caps are in the signal path, the required ADC input Vcm can be brought in at the junction of the two 26.7-Ω resistors (0.95 Vcm here).

The frequency response to the ADC inputs shows about ±0.3-dB flatness through 100 MHz (tuning this with the external Ctune), while the sense path at the balun output is a very near replica in shape with considerable attenuation. That measurement path loss is fine for response or harmonic distortion measurements. For lower-frequency spans, use the ADT1-6T.

This approach can be adapted to other design requirements, with the only requirement being a relatively large differential resistor at the ADC inputs broken into this differential-to-single-ended sense path structure. Reference 8 shows measured results using this circuit, revealing that fast Fourier transform (FFT) distortion performance is slightly better than the ADC-only specifications.

Once we have the single-ended version of the ADC input voltage available at the balun output, several harmonic-distortion measurement methods may be applied. Simple spectrum-analyzer measurement will get down to about −90-dBc levels, whereas source cancellation approaches will drop down to better than −110 dBc.[9]

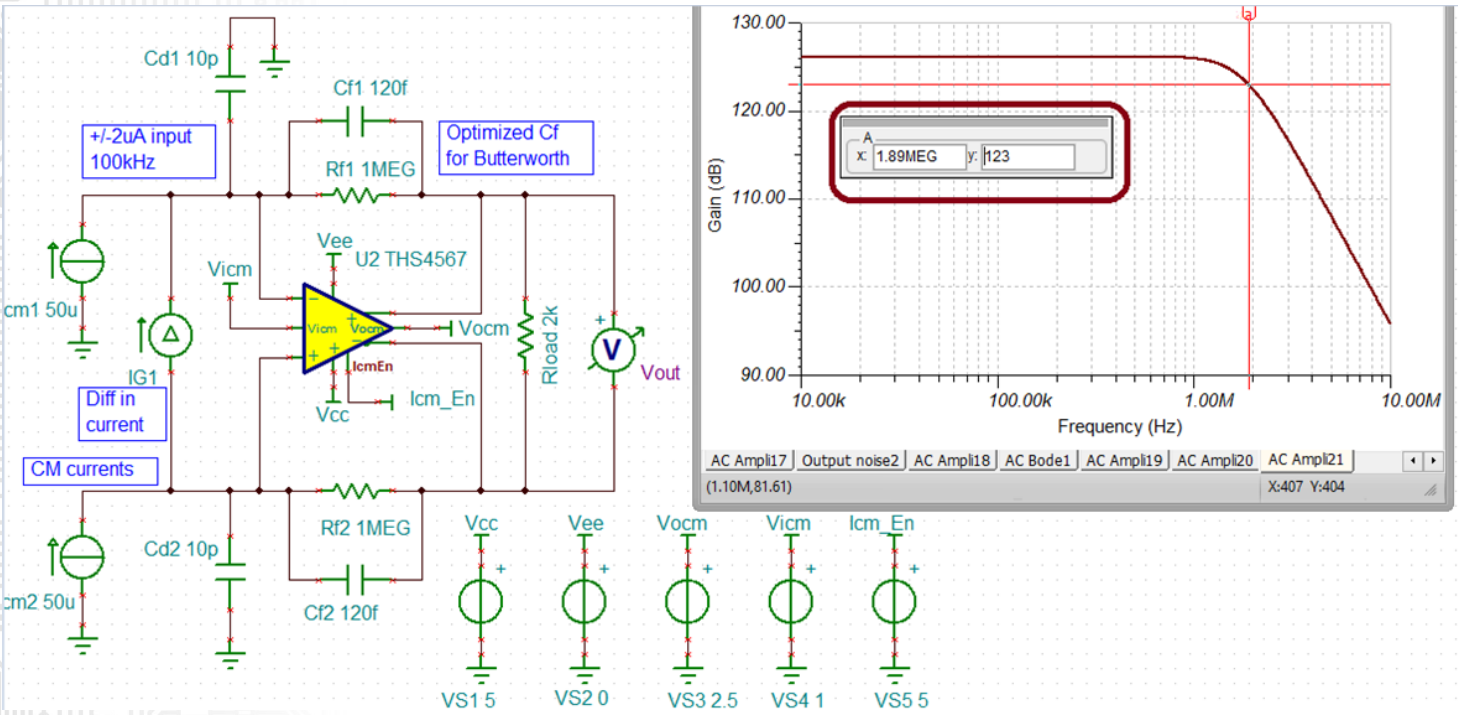
Legacy FDAs struggle with background CM signals on both inputs. A newer solution adds an input CM control loop along with the classic FDA design.

One of the more interesting problems that crops up occasionally is to implement a differential transimpedance stage instead of an FDA when the latter would seem to be applicable. Often, what's made this more problematic is if the two source currents have a large and varying CM current on top of the differential signal.

If that CM current is constant, sometimes we bleed that off at the input summing junctions with fixed resistors to some supply. That, of course, increases the dc noise gain and injects whatever noise is on the reference supply. And it won't work if that CM current varies with time.

The obvious, but previously unavailable, solution is to add an input servo loop that sums equal CM currents into the input nodes to hold an externally set "input" CM voltage. The new (released Dec. 2020) THS4567 starts out with a relatively fast 220-MHz, GBP decompensated core FDA structure and then adds this input servo loop to absorb the source CM current terms.

Since it's intended for differential transimpedance applications from detector diodes, the decompensated FDA is more suited to that application, where the first job in any design is to get the feedback Cf set for the desired frequency response, usually Butterworth. A simple



9. Frequency response for an optimized C_f for the 10-pF source capacitance design with 1 MΩ on each side.

solution for compensating a transimpedance design for the required feedback Cf to achieve a closed-loop Butterworth is as follows:[10]

First, get the approximate noise gain zero dropping out the feedback Cf from this equation for Z1, where Cs is the total capacitance on each input pin:

$$Z_1 = \frac{1}{2\pi R_f (C_s + C_f)} Hz$$

The characteristic frequency for the second-order closed-loop response will be given by:

$$F_0 = \sqrt{Z_1 GBP}$$

Where we need to be using the true single-pole GBP in this equation.[10]

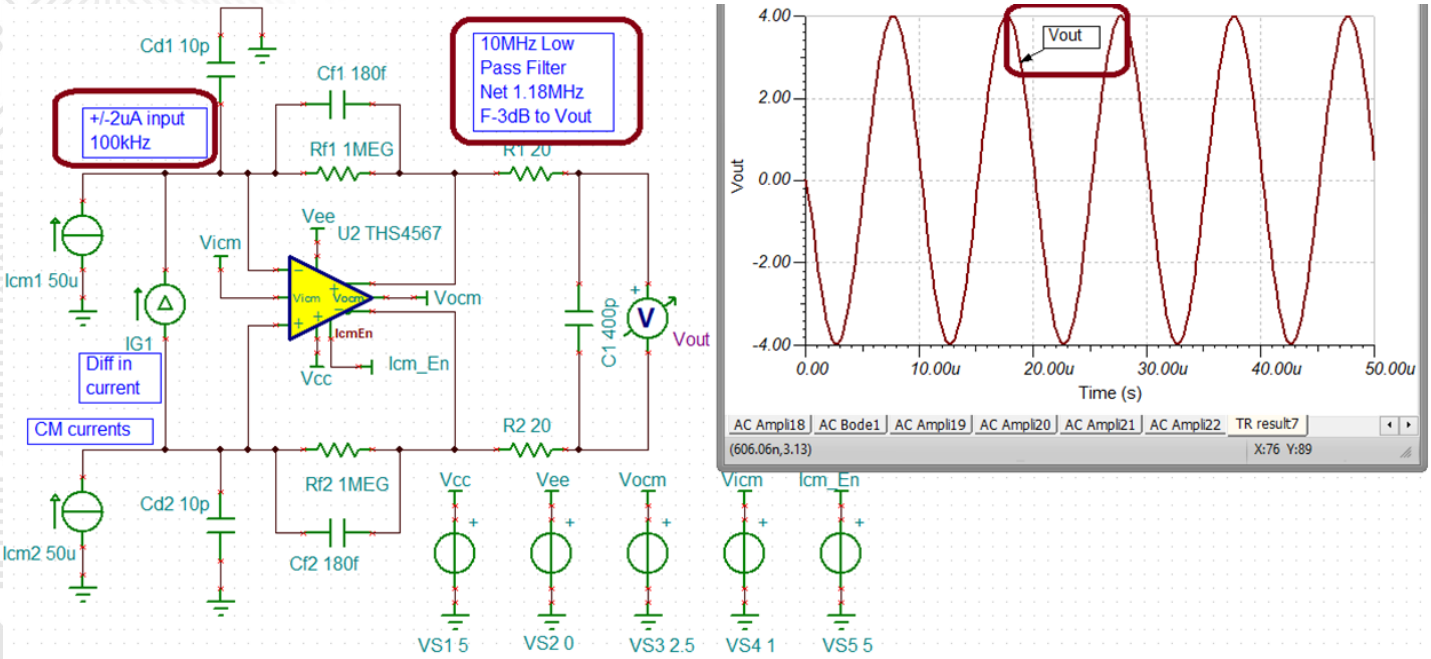
Then, to set the feedback pole location (P1), use this relationship, where F_c is the intersection of the higher frequency noise gain ($1+C_s/C_f$) with the GBP curve, but use the $P1/F_o$ part of this here:

$$Q = \frac{F_o}{F_c} = \frac{P_1}{F_o}$$

Setting P1 (the feedback pole) to get a Q = 0.707 (Butterworth) will then yield an F-3dB = F_o.

Stepping through this with a desired 1 MΩ on each side gain for the THS4567 with 10-pF detector diode capacitance will give:

Z1 = 1/(2π*1 MΩ*11 pF) = 14.47 kHz (where I've added 1 pF for the THS4567 input C on each side)



10. Full differential Zt design with 10-MHz postfilter showing ±2 µA at 100-kHz input.

F_o = √(14.47 kHz*220 MHz) = 1.78 MHz = F-3dB (if Q set to 0.707)

P1 = 0.707*1.78 MHz = 1.2 6MHz, Cf = 0.12 pF.

The response certainly looks Butterworth, with almost exactly the expected 1.8MHz F-3dB for this 2MΩ (126 dBΩ) design (**Fig. 9**).

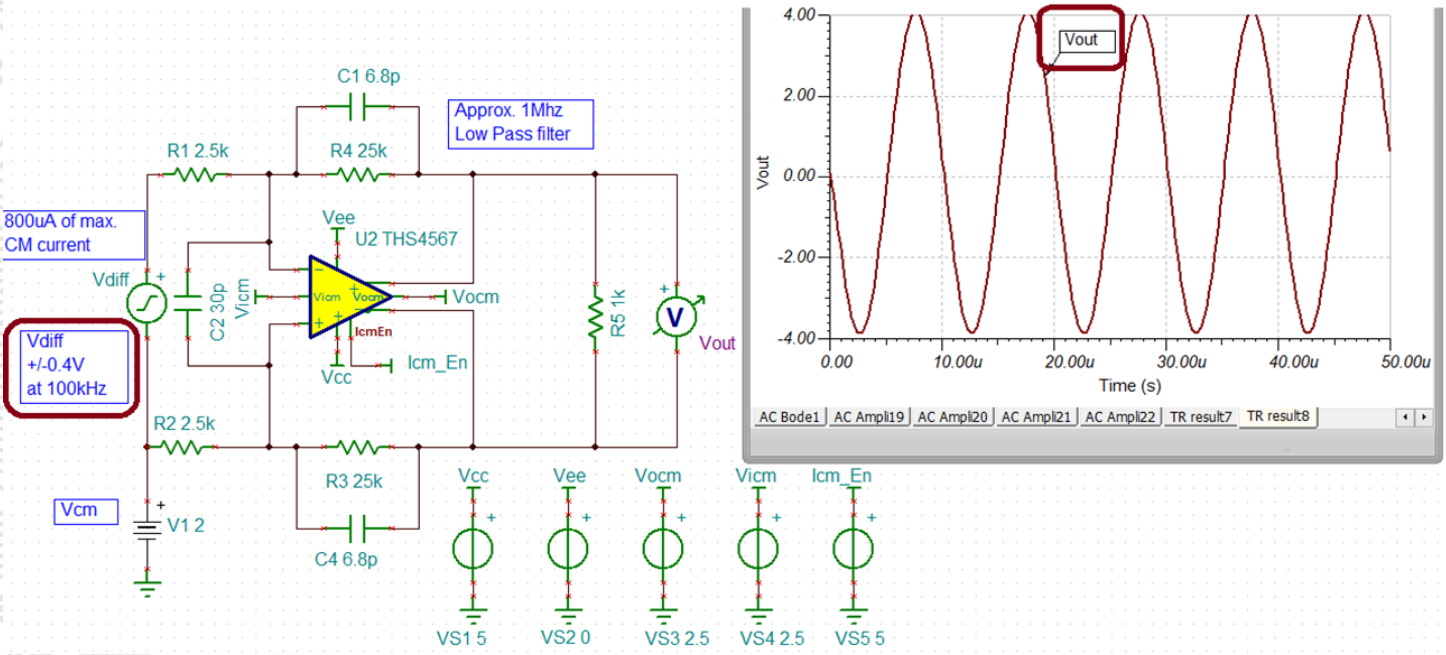
Resetting the feedback Cf to a typical thick-film resistor 0.18-pF parasitic, and adding a 10-MHz post RC filter, shows the ±4-V differential output of **Figure 10** for a ±2-µA, 100-kHz sine-wave input sitting on top of 50-µA CM input current. Without the input cancelling currents, that 50-µA CM current would be taking the outputs to negative 50 V.

Here, I had set the target input CM voltage to 1.0 V with the output Vocm midsupply at 2.5 V. Each output is swinging ±2 V around that to give the ±4-V differential output for the ±2 µA shown in Figure 10.

This device might also be used to gain up a small differential voltage signal on top of a larger CM source voltage that varies with time. In this case, the maximum input Icm current for the CM voltage range must be less than the maximum available internal Icm cancelling current. The specification doesn't appear in the datasheet, but up to 1 mA is supported in the simulation model.

Backing that maximum off to a safe ±800 µA maximum, use that to design a gain of 10 stage with ±2-V input CM range. That will then require a 2-V/0.8-mA = 2.5-kΩ input resistor with a 25-kΩ feedback R_f.

These higher R's will require some compensation. Here, I've added a feedback Cf to give a 1-MHz pole, then added a differential input C that will shape the noise gain to 10 V/V at higher frequency (**Fig. 11**).[12] The input Icm servo loop cancels the input 800 µA of CM current to hold the input pins at 1 V. Those two Icm currents do have some offset introducing an output offset voltage in this simulation.



11. Differential voltage gain of 10 V/V with ±2-V CM reject using the THS4567.

This brief survey of some of the newer results coming out of the various amplifier development groups just touch on the vast range of newer (and hopefully better) analysis approaches and devices that have emerged over the last 10 years. Many more exist, but they require a close reading of the vendor material to expand your horizons. Someday, most of these might appear in an updated textbook.

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11. Why is Gain Bandwidth Product so confusing?
12. Unique compensation technique tames high bandwidth voltage feedback op amps

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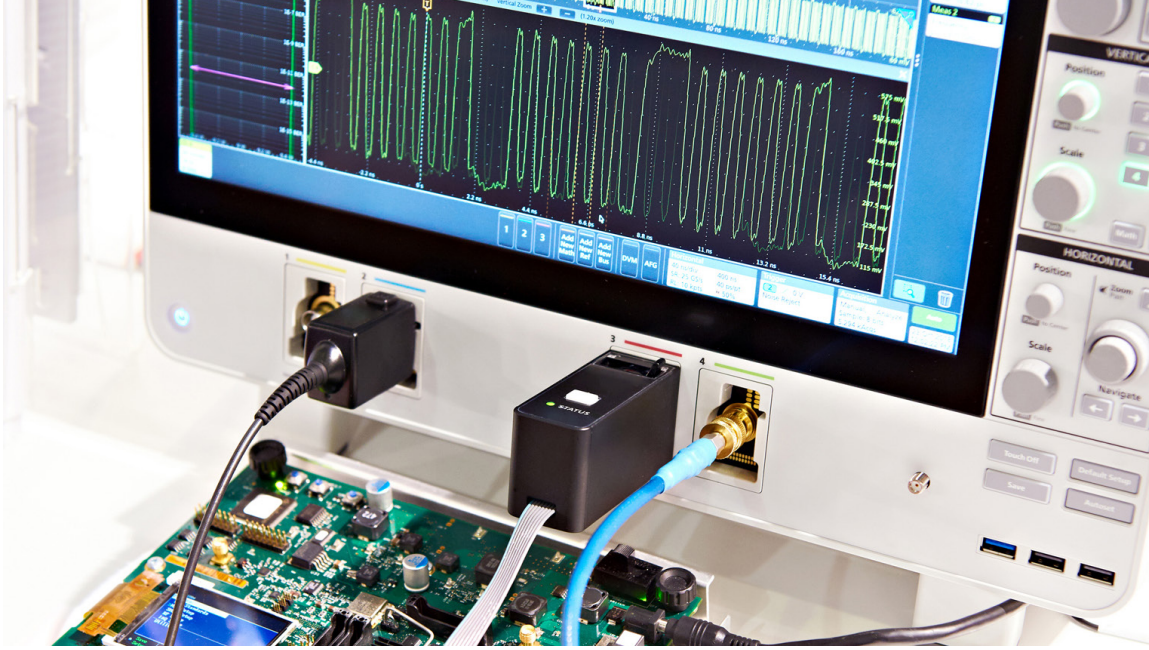

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CHAPTER 4:

What Are Analog Signal-Path Design Engineers Up To?

CABE F.S. ATWELL, Editor, *Electronic Design*

The median age of analog signal-path engineers continues to increase. Should we be worried?

Signal-path design refers to the process of designing the route or path that a signal (such as an electrical or optical signal) takes as it travels through a system or device. This includes the selection of components and their configuration, as well as the optimization of the signal path to meet specific performance requirements. The signal-path design process also includes factors such as signal integrity, noise, and signal loss.

A signal-path design engineer is a professional who designs and optimizes the route or path a signal takes as it travels through a system or device. Engineers within this field also may work with a variety of signal types, such as electrical, optical, and wireless signals. They may be involved in the design of a wide range of systems and devices, including communication systems, electronic devices, and medical equipment.

Furthermore, engineers in this field must have a good understanding of signal processing, electronics, and communication systems, in addition to knowledge of signal integrity, noise, and signal loss. On top of that, the engineer should be proficient in using various simulation tools and software packages to design and optimize signal paths.

Survey Says...

With that said, our recent *Electronic Design* survey paints signal-path design engineers by the numbers, with metrics that encompass everything from primary job functions to circuit types. The information provides a detailed overview of engineers working within the analog signal-path design field and what the future might hold for both new and veteran engineers.

Analog signal-path design is a specialized field within electrical engineering and typically requires a solid knowledge of circuit design and analysis and experience with analog components and systems. It's a relatively small field, as many designs are now digital.

The number and ages of actual engineers within this field from a global perspective are currently unknown. Though if we consider that the analog signal-path design is a subset of the electrical engineering field, the U.S. Bureau of Labor Statistics *Occupational Outlook Handbook* provides some less-than-stellar numbers.

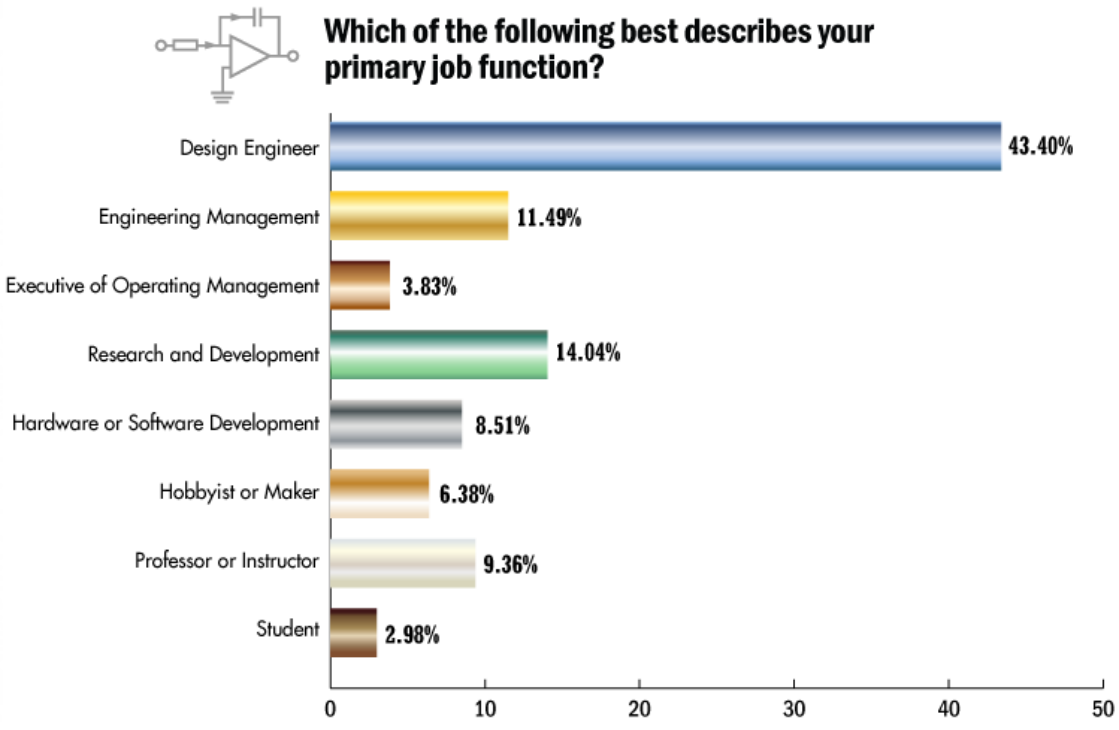
Overall employment of electrical and electronics engineers is projected to grow 3% from 2021 to 2031, slower than the average for all occupations. Despite that limited growth, about 20,100 openings for electrical and electronics engineers are projected each year, on average, over the decade. Most of those openings are expected to result from the need to replace workers who transfer to different occupations or exit the labor force, including retiring.

More Specifics in Job Functionalities

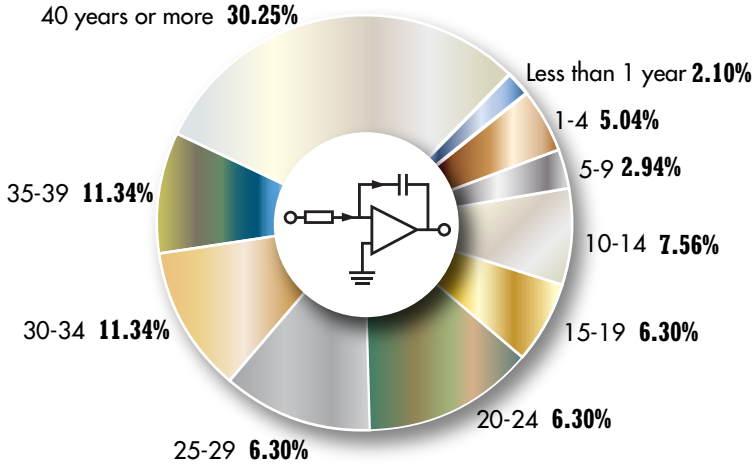
Analog signal-path design engineers often specialize in specific job roles depending on company requirements and needs that arise within a project scope (**Fig. 1**). Some are tasked with R&D, designing ICs from the beginning to end of a project lifecycle. Others can take on the mantle of management based on education and training, job history, and qualifications throughout their careers.

Most engineers in the field are involved with the design element, creating circuits and systems that are used to process signals in various applications, such as telecommunications, audio processing, and instrumentation.

Their role is to determine the best way to transmit signals from one place to another with minimal loss and interference. This requires a deep understanding of electrical theory, circuit design, and the properties of different components, as well as a mastery of specialized design tools and simulation software.



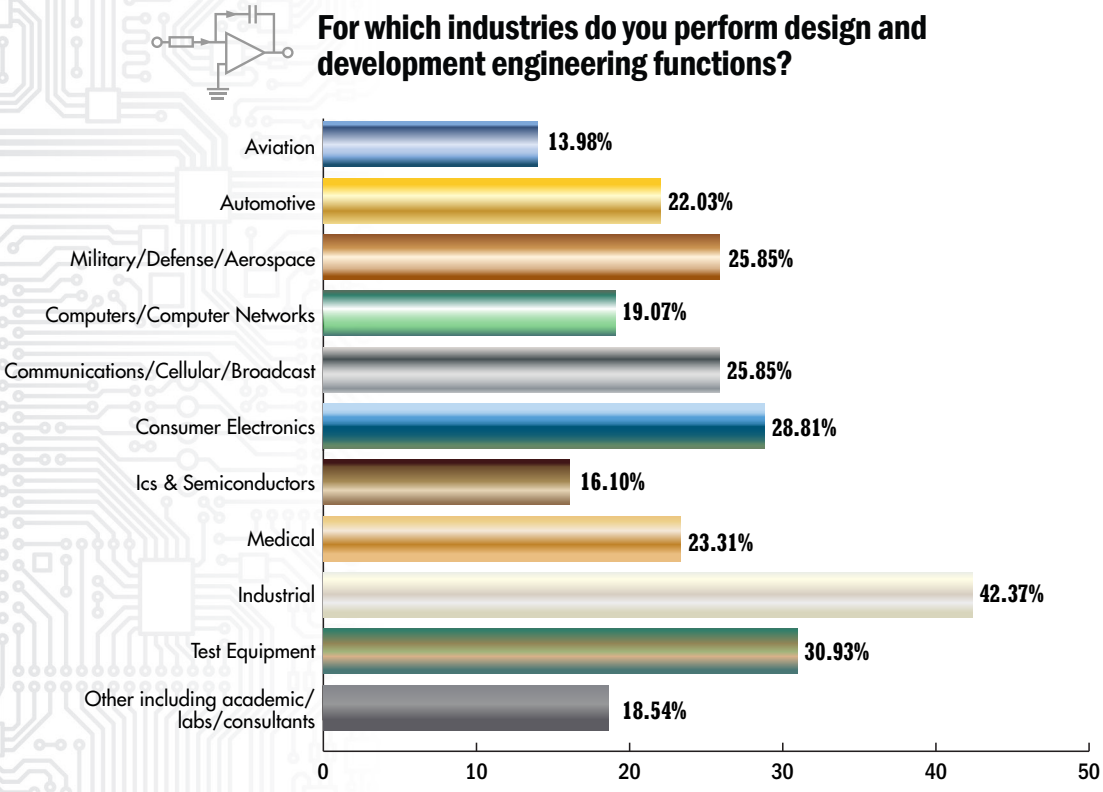
1. Design engineers topped the list of job functions in our survey.



2. Over 70% of the engineers surveyed had more than 15 years of experience under their belts.

The goal of an analog signal-path design engineer is to create efficient and effective signal-processing systems that meet the needs of the particular application, whether it's for consumer electronics, medical devices, or aerospace systems.

The most significant percentage of engineers have been in the industry for 40 years or more while dealing with the design element (**Fig. 2**). And because few new engineers are entering the field, it could have an impact on legacy designs that may be lost as veterans retire.



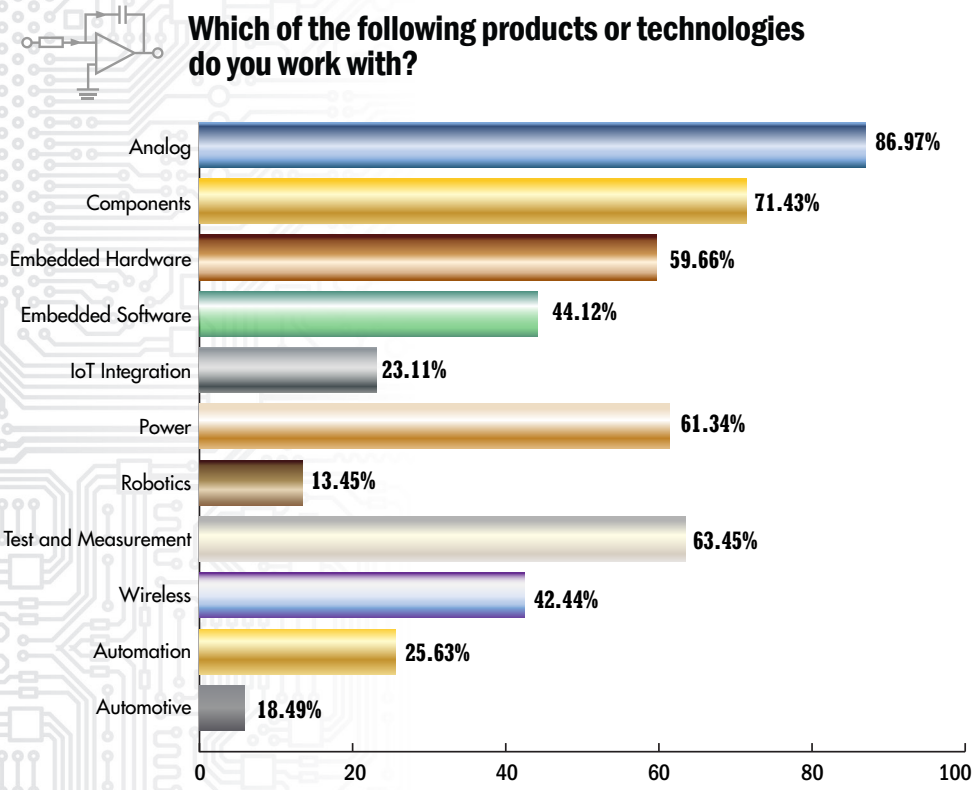
3. The engineers surveyed work in a broad range of markets.

Over 41% of those engineers work in an industrial environment, such as those in aerospace, automotive, medical, and defense (**Fig. 3**). Job functions in this area can include designing and implementing analog signal-processing systems for industrial control systems, testing analog circuits for industrial sensors, and integrating analog signal-conditioning circuits. Others are tasked with designing test equipment, consumer electronics, and communications systems.

No matter the industry, the highest percentage of analog signal-path design engineers today take advantage of a variety of component technologies through the design pro-

cess for any number of applications (**Fig. 4**). Some of the most commonly used analog technologies in signal-path design include operational amplifiers (op amps), comparators, and voltage regulators. Designs may require filters to remove unwanted frequency components from a signal, or to isolate a particular frequency band.

Engineers also can take advantage of analog-to-digital converters (ADCs), digital-to-analog converters (DACs), AM and FM circuits to modulate carrier signals, and conditioning ICs to refine signals for further processing (**Fig. 5**). These are just some of the many analog technologies commonly used by signal-path design engineers in their projects, which is often done two or more times per month.

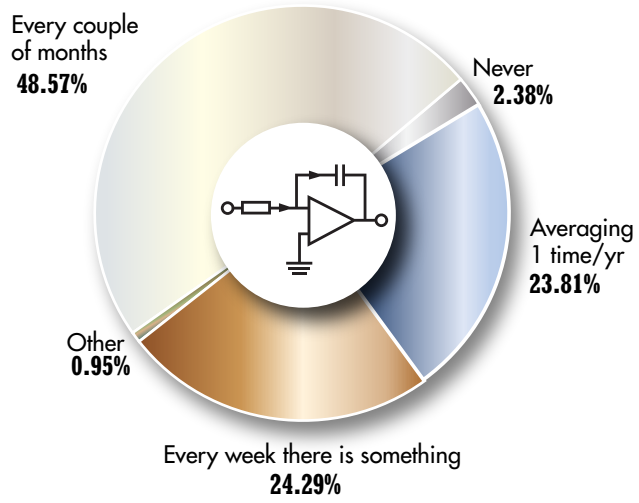


4. Power, test and measurement, and wireless are the main focuses of analog signal-path engineers.

Responsibilities

Of course, designs are regulated based on the area of work responsibility. According to the survey, engineers are tasked to design mixed signals and analog hardware every couple of months, followed by system designs and software development (**Fig. 6**).

This involves selecting suitable components and circuit designs and requires a comprehensive understanding of the signal-processing requirements, as well as a

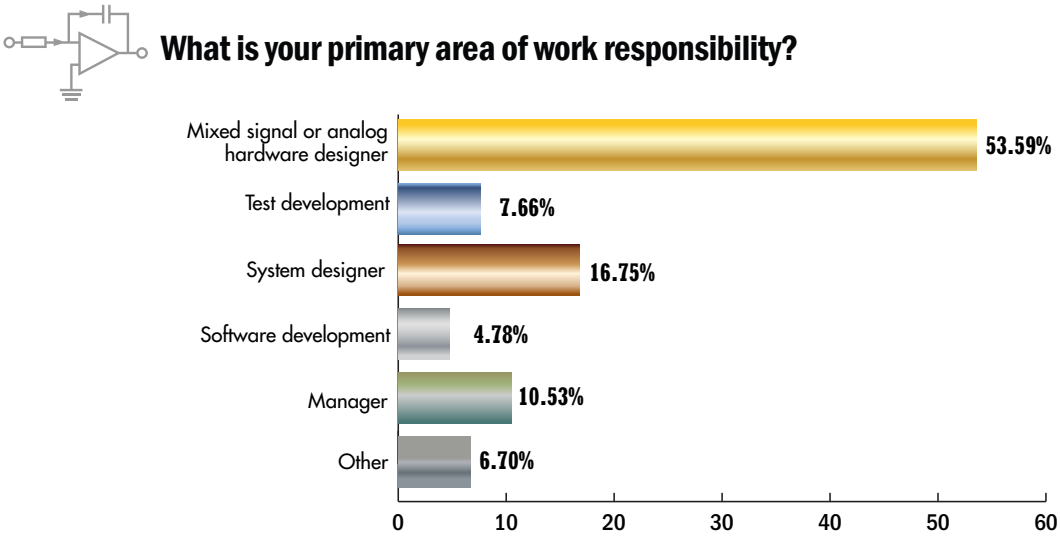


5. A signal-path designer typically is typically required to select a component or circuit design for an analog signal path once every few months or just once in a year.

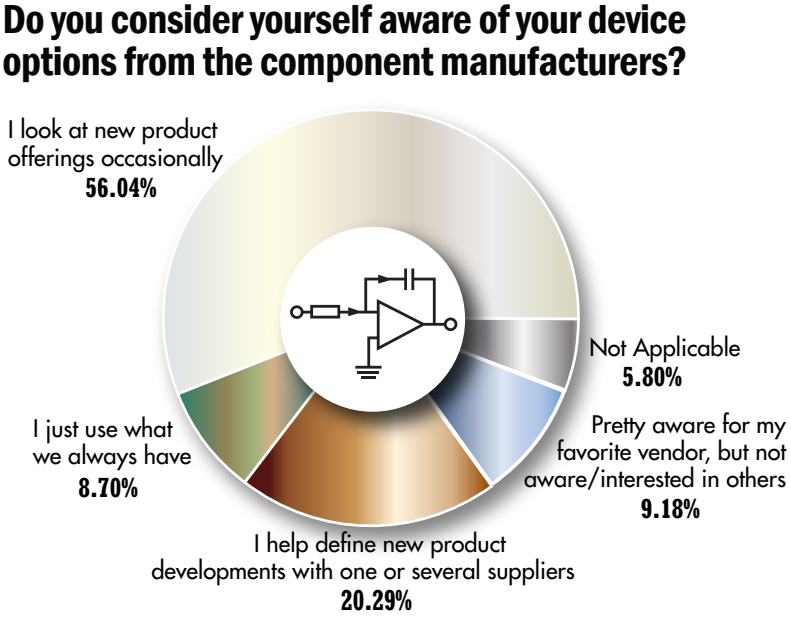
good understanding of the properties and limitations of various components. Component selection for those designs is usually dictated by the requirements and circuit topology, as well as voltage requirements, thermal characteristics, and other defining factors.

Most engineers in the industry are currently involved with analog signal-path design, the bread and butter within the field, and they're aware of the latest components and design elements from manufacturers (**Fig. 7**). This is often done via updated manufacturer product catalogs, vendor websites, subject-matter experts, and the latest press releases, which helps maintain awareness of current technologies as they become available.

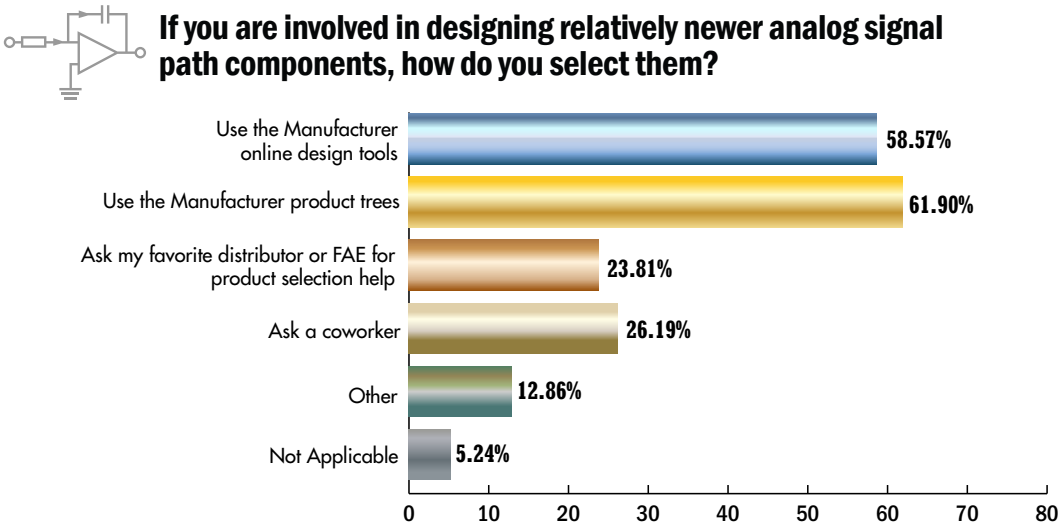
Moreover, the highest percentage of engineers typically use manufacturers' product trees and myriad online design tools to develop analog signal-path components (Fig. 8). Some of the most commonly used tools include circuit design and simulation software,



6. The majority of engineers admit they work in many different areas.



7. Most signal-path designers consider themselves aware of new technology.



8. Almost two-thirds of engineers rely on manufacturers to help them select components for newer analog signal-path designs.

component selectors and datasheets, technical reference libraries, online component distributors, and others. The right tool will depend on the specific requirements of the project and the resources available.

Conclusion

Analog signal-path engineers are essential in every industry. As shown in survey results, the number of analog engineers is dwindling. With few newer, younger engineers taking over those roles as others retire, a major crisis could cripple this venerable practice.

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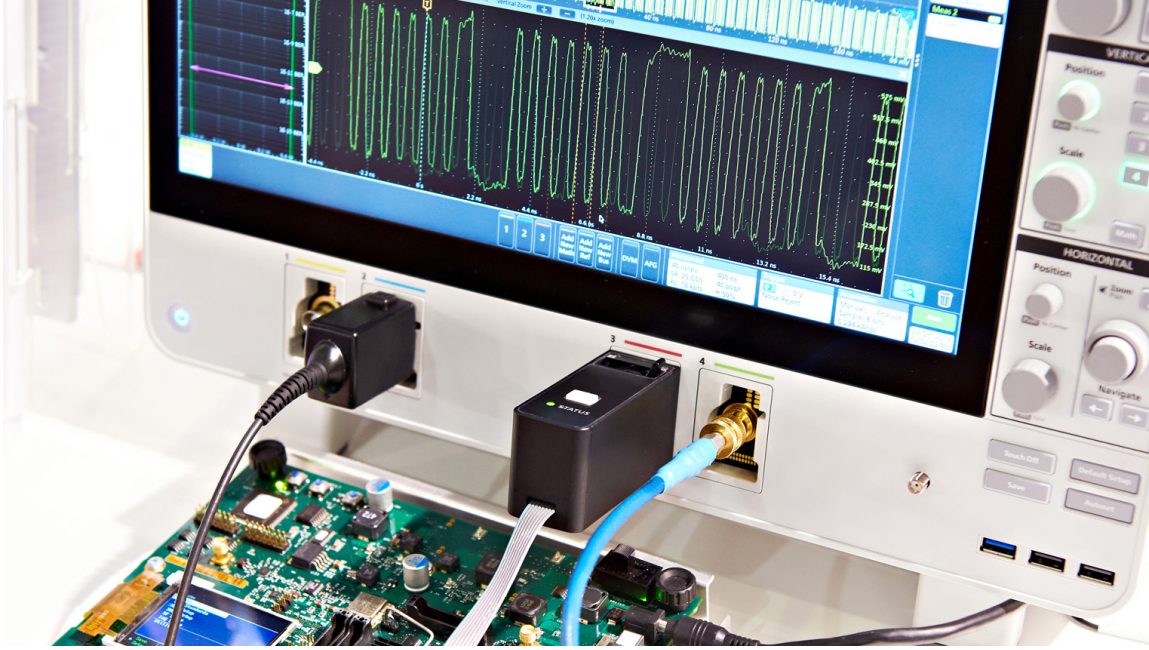

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CHAPTER 5:

The ABCs of Analog Signal-Path Design—and Coping with Today's Challenges

CABE F.S. ATWELL, Editor, *Electronic Design*

The state of analog signal-path engineering hasn't changed. Should we be worried?

Analog signal engineers specialize in designing, developing, and maintaining analog circuits and systems. The processing of analog signals is the manipulation of continuously varying signals, which are the opposite of digital signals that represent data as discrete values. Analog signals are still present in many electronic devices, including audio and video equipment, power supplies, and communication systems.

In this article, we will explore the role of analog signal engineers and the skills and knowledge required for success in this field based on a recent survey conducted by Endeavor Business Media.

So, What's Analog Signal Engineering?

Analog signal engineering involves designing and analyzing electronic circuits that process continuous signals. Analog signals vary continuously in time, and their value can take on any value within a range.

Examples of analog signals include audio signals, which represent sound waves, and video signals, which represent images. Engineers in this arena develop circuits that process these signals, such as amplifiers, filters, and modulators.

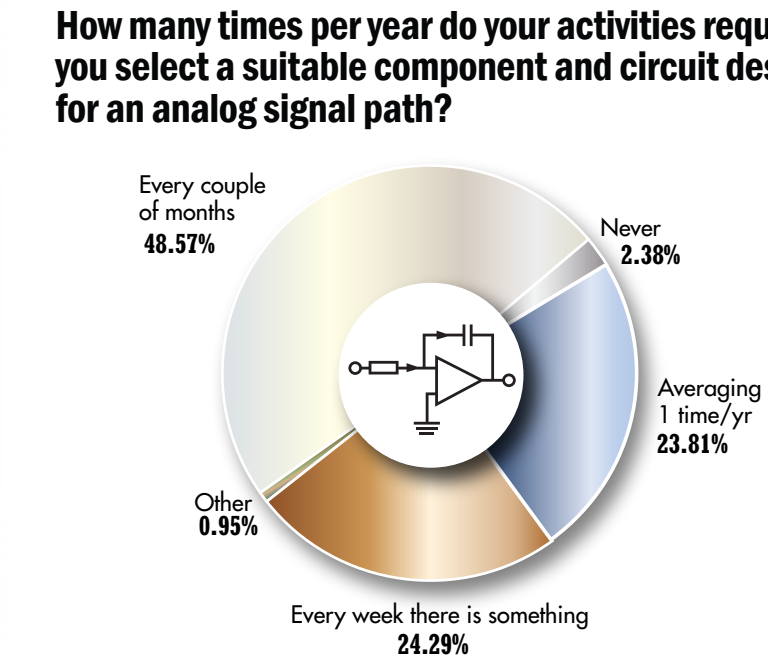
The field of analog signal engineering is closely related to other fields, such as power electronics, RF (radio frequency) engineering, and control engineering. Analog signal engineers must understand basic electronics principles, including circuit analysis, circuit design, and semiconductor physics. They also must be proficient in using simulation and analysis tools to design and optimize electronic circuits.

Most engineers within the analog field will typically create designs every few months,

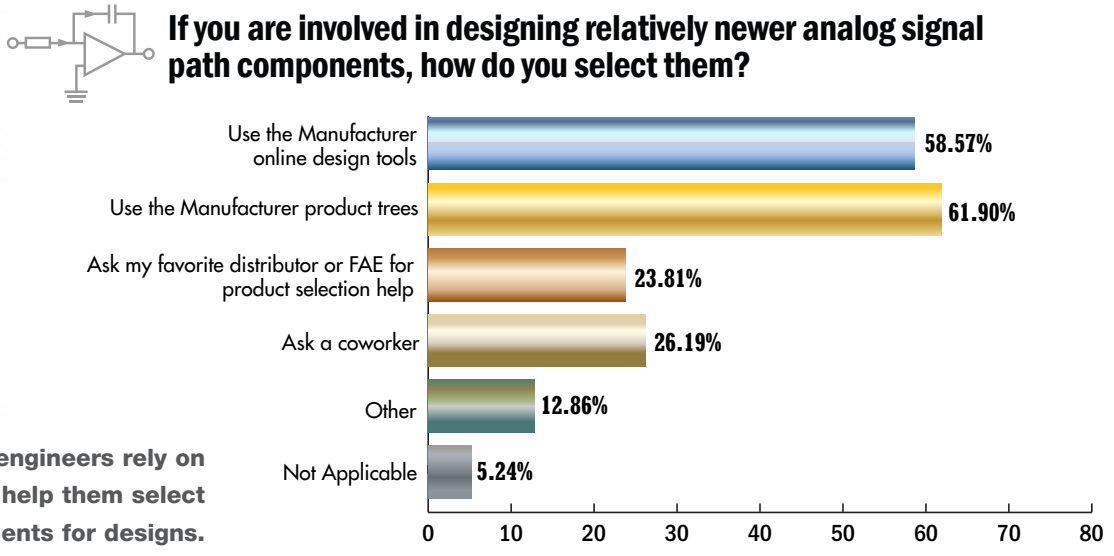
and that requires operational knowledge of components currently on the market (**Fig. 1**). Engineers often take advantage of various component technologies through the design process for any number of applications, and a working knowledge of the latest components helps simplify that process.

Among the most commonly used analog technologies in signal-path design are operational amplifiers (op amps), comparators, and voltage regulators. Designs may require filters to remove unwanted frequency components from a signal or to isolate a particular frequency band.

Many analog engineers are familiar with the latest components and take advantage of manufacturers' updated products via product trees, filters, and even tools integrated within some design applications (**Fig. 2**). The design flows and options available to engineers have never been greater, and most are up-to-date within their respective fields. To put that



1. The majority of engineers only select suitable components once every few months or less.



2. Most engineers rely on manufacturers to help them select newer analog components for designs.

into perspective, the flow for the analog signal-path design process generally involves the following steps:

1. *System-level requirements*: Define the overall specifications and requirements for the signal path, such as bandwidth, signal-to-noise ratio, and distortion.
2. *Circuit-level design*: Design the individual components of the signal path, such as amplifiers, filters, and modulators. This may involve selecting specific circuit topologies and component values.
3. *Simulation*: Use simulation software to verify that the signal path meets the system-level requirements as well as optimize the circuit-level design.
4. *Layout and fabrication*: Create a layout for the signal path on a printed circuit board (PCB) and fabricate the PCB.
5. *Testing and characterization*: Measure the performance of the signal path and compare it to the system-level requirements. Make any necessary adjustments to the design.

Some popular signal-path design options include:

Analog signal processing: This includes traditional analog circuits such as op amps, filters, and mixers.

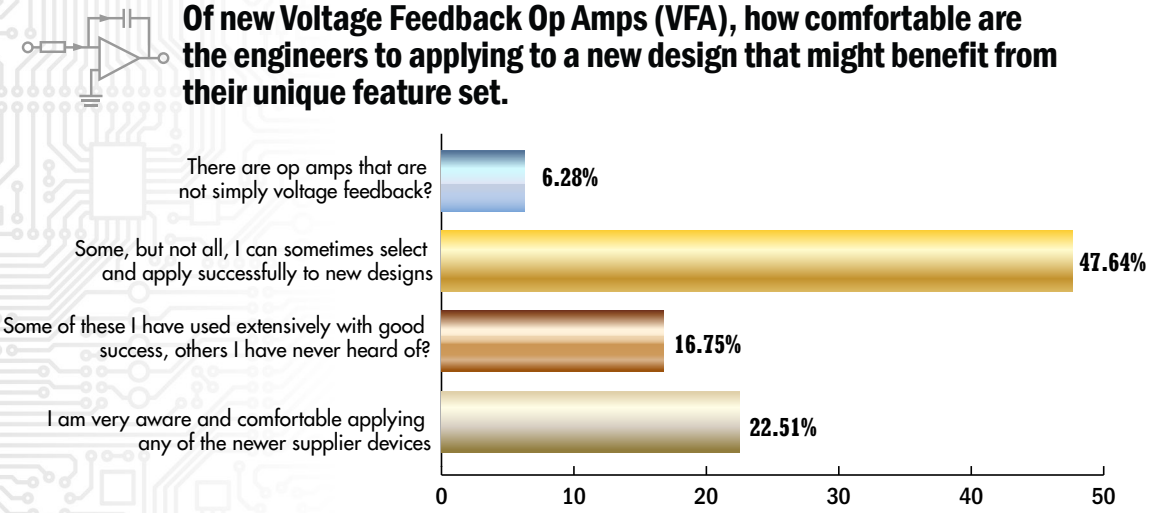
- *Digital signal processing*: Uses digital circuits and algorithms to process signals.
- *Hybrid signal processing*: A combination of both analog and digital signal processing.
- *Software-defined radio*: This uses a combination of analog and digital signal processing plus a microprocessor to implement a radio receiver or transmitter.

It's worth noting that some newer options include using machine learning and neural networks to process signals and utilizing integrated circuits (ICs) that integrate multiple signal-path components onto a single chip.

Component Selection

Selecting analog signal-path components also is crucial in designing and developing electronic circuits that process analog signals. Here are some essential factors to consider when selecting analog signal-path components:

- *Signal frequency*: The frequency range of the analog signal that the component will process is a key consideration. Some components, e.g., op amps, have a limited bandwidth and may not be suitable for processing high-frequency signals. Other components, e.g., inductors and capacitors, have a frequency-dependent response and must be selected based on the frequency range of the signal.
- *Signal amplitude*: The amplitude range of the analog signal is another important consideration when selecting components. Some components, e.g., amplifiers, must be selected based on their ability to process signals with a specific amplitude range. Other components, e.g., resistors and capacitors, may have a limited voltage or current rating and must be selected based on the signal amplitude.
- *Noise*: Noise is an unwanted signal that can degrade the performance of electronic circuits involved in processing analog signals. Components such as op amps and transistors can contribute to the noise in the signal path. When selecting components, it's essential to consider their noise characteristics and select components with low noise levels.
- *Linearity*: Linearity is the ability of a component to accurately reproduce the input signal without distortion. Components such as amplifiers and filters must be selected based on



3. Almost all engineers are aware of VFAs and comfortable with selecting them for their unique features.

their linearity characteristics to ensure accurate signal processing.

- *Power-supply requirements*: Some components, e.g., amplifiers and voltage regulators, require a specific power-supply voltage and current. It's essential to consider the power-supply requirements of components when selecting them to ensure that the electronic circuit can operate correctly.
- *Temperature range*: Components can have a temperature-dependent response, and their performance may vary over a range of temperatures. When selecting components, it's important to consider the temperature range of the electronic circuit and select components that can operate correctly over that range.
- *Component availability*: Finally, it's essential to consider the availability of components when selecting them. Some components may be expensive or difficult to obtain, which can impact the overall feasibility of the electronic circuit.

Selecting analog signal-path components requires careful consideration of the signal frequency, amplitude, noise, linearity, power-supply requirements, temperature range, and component availability. By carefully selecting components that meet these criteria, analog signal engineers can design and develop electronic circuits that accurately process analog signals (**Fig. 3**).

The Venerable VFA

One of the more widely used components when designing analog devices is the original voltage feedback op amp (VFA). VFAs are a type of electronic amplifier used in a wide range of analog-signal-processing applications. These op amps have a voltage input and output and are typically used for applications that require high-gain amplification and precision signal processing. In a VFA, the input voltage is applied to the inverting or non-inverting input of the amplifier.

The op amp amplifies the input voltage by a specific factor known as the gain, which is determined by the feedback network. The op amp's output voltage is then fed back to the input through a feedback resistor, which stabilizes the gain and improves the amplifier's stability.

One of the key advantages of VFAs is their versatility. They can be used in various applications, including analog signal processing, signal conditioning, active filters, oscillators, and

voltage regulators. They're also relatively simple to use, with most op amps requiring only a few external components to configure them for a specific application.

However, some limitations to voltage feedback op-amps also must be factored in. For example, they may have limited bandwidth or gain accuracy when used in certain applications. In addition, they may be prone to oscillation or instability if the feedback network isn't properly designed.

Signal conditioning is a process engineers use to manipulate an input signal to make it suitable for measurement or control system processing. This typically involves amplifying, filtering, or modifying the signal to improve its quality or make it compatible with the system's requirements. Signal conditioning is often used with current-sense circuits and instrument amplifiers to amplify small signals and monitor power.

In a typical current-sense circuit using an instrumentation amplifier, the shunt resistor is placed in series with the current path, and the instrumentation amplifier amplifies the voltage across the resistor. The output of the amplifier is then processed by a filter or other signal-conditioning circuit to remove any unwanted noise or distortion and provide a clean, accurate measurement of the current.

Depending on the application, signal conditioning also may require using analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) to alter the signal. Most engineers will utilize legacy voltage feedback using current-feedback op amps and fully differential amplifiers. Signal processing leading up to an ADC typically involves several steps to prepare the analog signal for conversion, including filtering, amplifying, and holding a signal at a constant level before deployment.

Signal processing leading away from a DAC is similar to ADCs, although the signal needs to be shaped to match the requirements of the analog device. The signal also may need conditioning before entering the output stage to provide a specific frequency or amplitude response. This can be done using current fully differential amplifiers, and in some cases, higher input voltages.

Conclusion

Analog signal design engineering is a challenging and rewarding field that requires a strong educational background, a broad set of skills, and a dedication to staying up-to-date with the latest advances in circuit design and signal processing. Although engineers within the analog signal-path design field may find themselves in the minority, those numbers could change over the next decade as legacy systems continue to be a mainstay in the development process.

The future of analog signal-path design will likely involve continued advances in technology, such as using more advanced materials and fabrication techniques and incorporating digital signal processing (DSP) into analog signal-path design.

Furthermore, there may be a greater focus on designing for specific applications, such as medical imaging, communications, and automotive systems. The use of machine-learning algorithms and artificial intelligence could also play a role in the future of analog signal-path design, helping to optimize and improve the performance of analog signal-path circuits.

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