Electronic Design

By AKBER ROY, CEO, Rush PCB Inc.

Designing Noise-Free, High-Speed PCBs

High-speed circuit boards operating above 300 MHz can be a challenge when noise comes into play.

It's getting more difficult to design noise-immune circuits for several reasons: An increase in integration of components due to surface-mount technology; new package designs for these integrated circuits that bump up the number of pins per package; and miniaturization of components.

Such features lead to less distance between the conductors, which raises the values of capacitance and inductance per unit length of interaction. Consequently, it increases the induced interference in adjacent conductors.

One remedy is to boost the speed of signal circuits of modern PFs as well as have a large spread in speed, from 1 MHz to hundreds of MHz, and even 1,000 MHz. For example, there are circuits that transmit a signal at a frequency of 48 MHz and at 576 MHz.

The increase in speed decreases the duration of the signal front, which, in turn, leads to problems in ensuring the integrity of the signal during its transmission. With a large spread in the speed of signal circuits, one needs to classify communication lines and evaluate their noise immunity.

Routing and Modeling in High-Speed Circuit Boards

From these features, it follows that in the early stages of design, both for routing and modeling, it's necessary to allocate transmission lines with common routing rules. To do this, you need to create a pre-topological analysis procedure.

Moreover, a post-layout analysis procedure is required, i.e., a topology-checking mechanism to identify and correct PCB layout errors.

The concept of noise immunity is complex. It includes protection from external and internal pickups. This article discusses internal noise immunity.

Noise immunity of electrically short communication lines was considered according to the active-passive line model, or active-passive-active, involving minimization of interference reflections for differential transmission lines and for electrically long transmission lines. The elimination of interference in power circuits was taken into account, too.

Fixing Noise Issues in High-Speed PCBs with Altium Designer

The solution to these problems can be combined into a single technique, which includes algorithms for pre-topological and post-topological analysis.

The technique is geared to the Altium Designer package—i.e., the forced limitation of the length of conductors and the area of interaction of two or more conductors—and the HyperLynx package for checking the resulting topology. The TXline package calculates differential transmission lines *(see figure)*. The need to use various software products is due to their advantages in different areas of design.

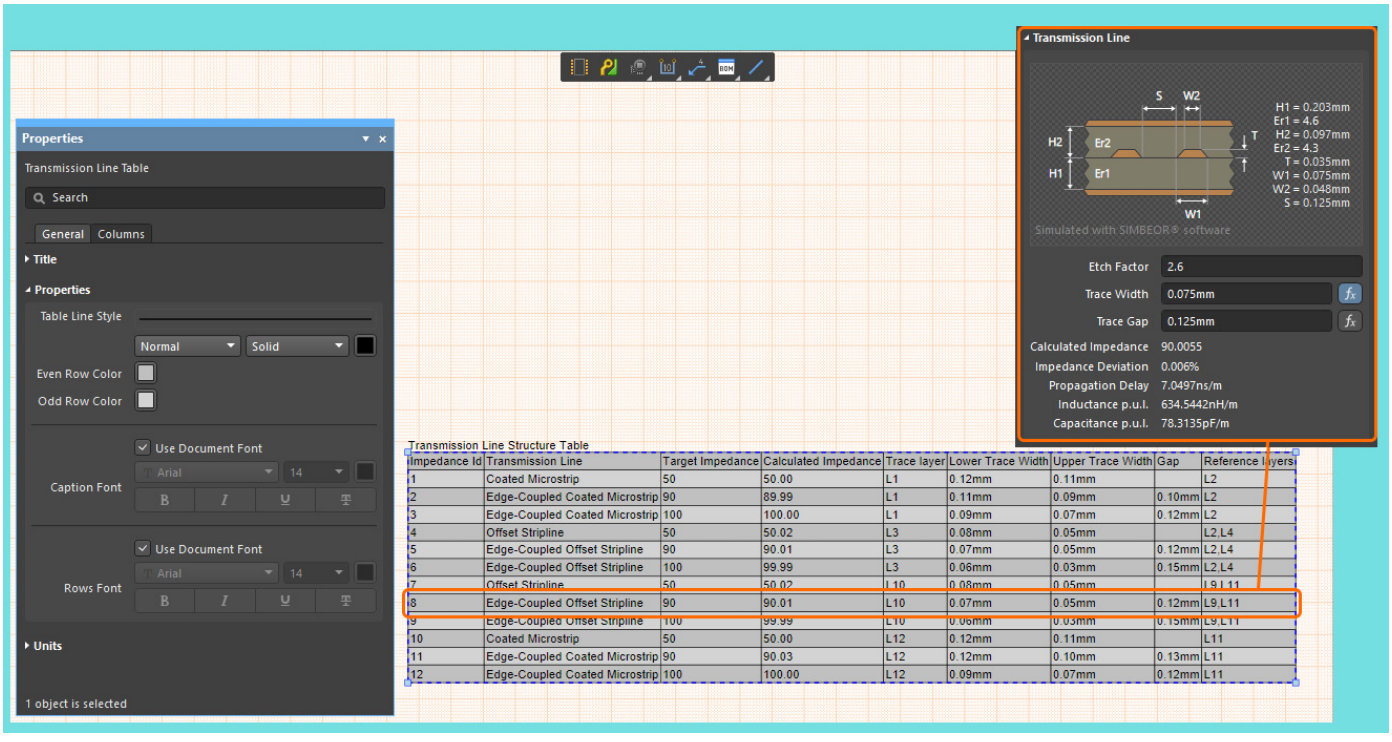
Based on the developed methodology, the circuit board of the CF subunit was designed and tested. The digital filter subunit and its circuit board can be classified as high-speed equipment, since its circuits include circuits that transmit a signal with a frequency above 300 MHz.

Design Methodology

The task of the pre-topological analysis of the noise immunity of the FYa TF and the choice of the layout of elements forms the criteria and rules for interactive routing of a PCB, which is resistant to external and internal interference (electromagnetic and electric fields).

The initial data for pre-topological analysis are the electrical circuit diagram, element parameters (for example, number of pins, pin pitch), characteristics of the entire device (for example, supply voltage), and noise-immunity values of microcircuits.

Based on the expected area of the board and the expected volume of the product and other design features, the size of the PCB is determined. Then, based on the expected number of connections on the PCB and the parameters of the microcircuit packages, the pitch between the conductors and the accuracy class of the board is determined.



Altium Designer's TXline package can calculate differential transmission-line configurations.

Factors to Consider in High-Speed Circuit-Board Fabrication

From the parameters of the device, namely, the supply voltage, we determine the number of layers of the developed multilayer printed circuit board (MPC).

After analyzing the electrical circuit diagram, we sort all of the circuits so that the frequency of the transmitted signal between groups differs by about 10X. Subsequently, the average length of the connection *l* is determined, on the basis of which we will classify the transmission line as electrically long or electrically short.

For an electrically short transmission line, additional matching of the line with the load and signal source isn't required. The voltage at all points along the length of the line at a certain point in time has the corresponding identical values.

Short lines are modeled by lumped ideal elements; their typical models are electrical capacitance or inductance. For electrically short transmission lines, the level of crosstalk must be determined.

Evaluate the Level of Crosstalk

For electrically long communication lines, it's also necessary to evaluate the level of crosstalk at the beginning and end of the line. Based on the level of interference and the values of the crosstalk coefficients at the beginning and end of the line—the pulse front—select the required distance between the conductors and the length of the allowable interaction section.

For these transmission lines, typically one must find not only the values of the linear capacitance and inductance of the communication line of two conductors, but also the intrinsic capacitance and inductance of each conductor. Eventually, it will be required to choose whether or not to match the transmission line with the signal source and with the load.

Interference in the power supply and grounding system (consumption current surges) can be eliminated by reducing the resistance, namely the inductance of the power bus. Particular attention should be paid to the installation of decoupling capacitors on the board to power the IC. The capacitors protect microcircuits from power surges.

Follow these rules when laying out decoupling capacitors on the MPP:

1. Place decoupling capacitors as close as possible to the power and ground pins of the microcircuits.

2. Wide, short conductors should be used between the plated hole and the pad of the capacitor.

3. The plated hole should be next to the pad, or directly in the pad (microvia).

4. If the metallized vias of decoupling capacitors carry currents opposite in direction, then these holes should be located at the minimum possible distance from each other (preferably no more than *l* mm).

It's possible to reduce the inductance of the power supply and grounding system by properly forming the MPP structure. The power layers and return layers (ground layers) must be placed as close as possible to each other so that the capacitance of the resulting planar capacitor is larger (which, in turn, leads to a decrease in the inductance of the power supply and ground).

The formation of the MPP structure will further simplify the task of assessing its noise immunity.

The power and ground conductors should be as wide and

short as possible. We will determine the width of the conductors based on the values of the current flowing through the conductor and the allowable voltage drop on the power bus.

Now let's go to the analysis of transmission lines of information signals. By selecting any of the formed groups, we determine the critical length of the communication line (l_{KP}). If the ratio $l/l_{KP} \leq 0.5$, then this transmission line can be classified as electrically short. If $l/l_{KP} > 0.5$ and < 0.9, the given transmission line is neither electrically short nor electrically long.

With this technique, for such transmission lines, it's possible to increase the signal's minimum edge by introducing additional elements (resistors or capacitors) into the circuit in case the crosstalk value doesn't satisfy the condition.

It's important to remember that an increase in the front must be agreed upon with the developer since this degrades circuit speed. If $l/l_{KP} > 0.9$, the transmission line is electrically long. For electrically long transmission lines, designers must set the characteristic impedance and determine the margin of the transmission line's internal noise immunity. By choosing the parameters of the transmission line, the specified and calculated wave impedances must be equal.

Level of Crosstalk from Neighboring Conductors

If the wave impedances are equal, we proceed to analyze the crosstalk level from neighboring conductors and options for matching the transmission line with the signal source and load.

Differential transmission lines transmit high-frequency signals so that they can be attributed to electrically long communication lines. Next, set the differential wave impedance and determine the margin of the transmission line's internal noise immunity.

Before designing, it's necessary to determine the type of the differential transmission line. For example, is it a strip line or microstrip line? The advantage of striplines is that mode velocities are the same and there's no interference at the far end of a passive line (unlike a microstrip line). However, using surface mounting for the stripline requires vias.

The effect of this on transmitting differential signals must be evaluated with special software tools. And it's necessary to evaluate all of the advantages and disadvantages of one or another option and choose the most suitable for the design being developed.

Parameters of the Differential Transmission Line

Set the differential transmission line's parameters (distance between conductors, conductors' width, and distance between the conductors and the screen layer). For the given parameters, calculate the differential wave impedance.

If the value of the calculated impedance and given impedance are the same, calculate the level of internal noise and transmission-line length. To eliminate skew when transmitting a differential signal, calculate the allowable difference between the conductors' lengths in the communication line.

Method for Matching the Designed Transmission Line

The final step is to choose a method for matching the designed transmission line with the load and signal source. In some cases, if there's a difference in the design of one line of the differential pair, an alternating component may appear in the general signal.

In this case, it's necessary to coordinate the differential signals and general signal, which can be done with a with a U- or T-shaped switching circuit.

Pre-topological analysis of the FY CF yields a set of parameters of various communication lines, which at this stage provide noise immunity for the product, the minimum crosstalk values, and good traceability of the entire circuit. These parameters let engineers correctly arrange elements on the PCB.

If some communication line's parameters lines aren't available during routing (e.g., the length of the interaction section of adjacent conductors), the PCB's parameters must be adjusted. For example, increase the number of signal layers. Then, in accordance with the selected parameters, recalculate the wave impedances of the line's gears.

Post-Topological Analysis

Post-topological analysis checks the fulfillment of specified rules for the design of PCBs and parameters of printed conductors.

Initial data for this analysis is the finished topology and parameters of the transmission lines calculated earlier. Since Altium Designer doesn't allow for interactive control of the transmission lines' lengths, report the lengths of all conductors and compare them with previously calculated ones.

For differential-signal transmission lines, it's necessary to monitor the lengths and control the difference between the lengths of conductors in a pair to eliminate skew. If any conductor exceeds the allowable length, the circuit's topology must be corrected.

Troubleshooting methods:

- Partially rearrange the circuit elements. It's possible to shorten the interaction section and the conductor.
- Reroute the conductor. It should be placed further from the offending conductor.
- If there's not enough space to reroute the conductor, it can be moved to another signal layer.

After tracing and manually checking the topology, export it to HyperLynx. To evaluate crosstalk and the critical link

length, designers must do an automatic quick analysis, a fast analysis technique based on an expert algorithm.

An expert algorithm that identifies crosstalk nets makes worst-case assumptions so that no crosstalk nets are missed. This means the Standard IC Model is used if no transmitter model is in the circuit. Also, the algorithm assumes all chains are inconsistent.

The sum of the intensity of the two strongest aggressors also is displayed in the report file, as this is the most typical. To generate the Crosstalk Strengths Report, an expert algorithm uses the transmitter edge speed and the transmission-line interference information.

It's necessary to set those values that were determined earlier, at the stage of pre-topological analysis, and which represent the worst case. In the HyperLynx window, you can see the area containing the problematic circuits.

Summary

The advantage of the technique presented here is that it allows you to develop a board with any value of noise immunity. While verifying the topology in the quick-analysis procedure, designers can reduce the allowable amplitude of crosstalk amplitude, thereby letting the board meet quality goals.

Akber Roy is CEO of Rush PCB Inc. with *20 years of experience in electronic contract manufacturing.*