STEVE TARANOVICH, Contributing Editor

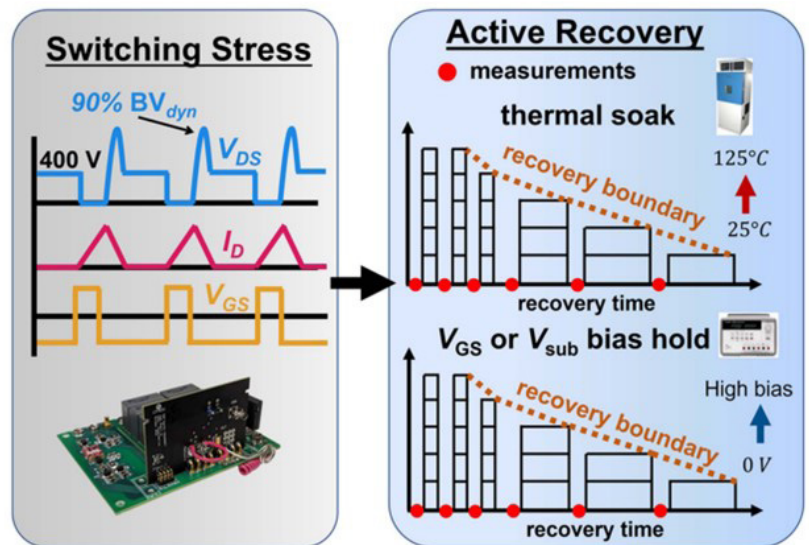# GaN Overvoltage Effects: Degradation and Recovery

This article presents a comparative study of the parametric recovery and shift of three mainstream GaN HEMTs experiencing repetitive overvoltage switching close to their dynamic breakdown voltage.

allium-nitride (GaN) high electron mobility transistors (HEMTs) have a limited avalanche capability. Thus, they may frequently experience catastrophic failures in voltage overshoot up to their dynamic breakdown voltage (BV_{dyn}).[1] Unfortunately, some very critical application-oriented knowledge gaps remain for the overvoltage ruggedness of GaN power HEMTs *(Fig. 1)*.

The ongoing activity of GaN power HEMT device recovery after an overvoltage stress and the recovery acceleration event are critical for device users; however, their recovery remains unknown. An appreciable change in internal carrier dynamics may occur in GaN power HEMTs at an overvoltage/surge approaching BV_{dyn}.

For any given GaN HEMT device, a supplier must determine its potential use conditions ranging from manufacturing to shipping to the end-user. In addition, its exposure to environmental settings in its useful life (indoor and outdoor) must also be examined. System and application stress, and lifetime requirements, must be observed as well.

Subsequently, a failure modes and effects analysis (FMEA) will need to be created that combines the collected knowledge of device behaviors and possible (failure/degradation) effects when stress and other factors are considered. To aid

1. The general methodology of this failure, degradation, and recovery study consists of repetitive overvoltage switching, followed by a variant of natural or active recoveries. (Image courtesy of Reference 1)

in creation of the FMEA, JEDEC published [JEP131](#) ("Potential Failure Mode and Effects Analysis–FMEA").

GaN HEMT Degradation

GaN HEMTs can be influenced by various degradation mechanisms that aren't observed in silicon or gallium-arsenide (GaAs) devices because of operating conditions under higher current densities, higher temperatures, and electric fields. Within such environments, GaN HEMTs may experi-

ence degradation with the possibility of catastrophic failures.

Material properties, like piezoelectric effects, occur with heteroepitaxy (this is a type of epitaxy performed with materials that differ from each other). In heteroepitaxy, a crystalline film is grown on a crystalline substrate or film of a different material. This technology is typically applied in cases where crystals can't otherwise be obtained (to fabricate integrated crystalline layers of different materials) on silicon-carbide (SiC) or Si substrates, thermal interfaces with packages and substrates, and higher densities of deep-level defects.

Most of the degradation-related effects are able to be traced, measured, and analyzed by electrical performance testing. Nevertheless, as compared with the continuous degradation processes, catastrophic failures are instantaneous and difficult to analyze with common electrical measurements. Thus, more attention can be drawn by performance instability research and long-term reliability instead of physical analyses of post failures, which are significant in reliability improvements of GaN HEMTs.

The most stressful GaN test regimes are: [5,6,7]

1. Off-state: high vertical and lateral field (dielectric failure, GaN TBD)

2. Hard-switching: self-heating and hot electrons

3. On-state: positive gate, p-GaN, or gate dielectric degradation

Time-Dependent Dielectric Breakdown Issues

GaN devices have no dielectrics, but semi-insulating GaN behaves like a dielectric. Failures in GaN are Weibull-distributed.[9]

Time-dependent dielectric breakdown (TDDB), which is under constant voltage stress (CVS) of GaN power devices, are subjected to positive and negative substrate biases that have been evaluated experimentally. These experimental results, along with statistical analysis of GaN power devices' TDDB under different substrate biases, have been studied.[10]

The Weibull shape parameter β will indicate if the failure rate is increasing, constant, or decreasing. Therefore, if $\beta < 1$, the system or component will have a decreasing failure rate. This kind of scenario is a typical sign of "infant mortality"
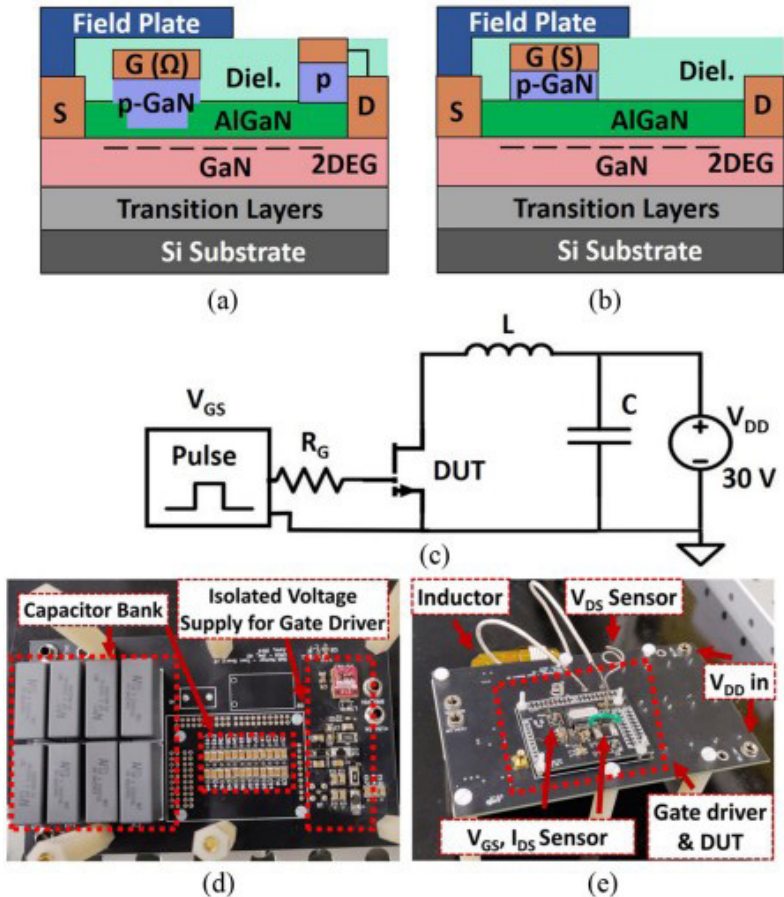
2. Shown are the schematics of (a) GaN hybrid-drain gate injection transistor (HD-GIT), (b) GaN SP-HEMT, and (c) the unclamped inductive switching (UIS) test circuit developed in Reference 12. The photos depict the (d) motherboard and (e) daughterboard. (Image courtesy of Reference 11)

and indicates whether the system or component is failing during its "burn-in" period. If $\beta = 1$, there will be a constant failure rate.

Less electron injection, from depleted two-dimensional electron gas (2DEG), will result in a monotonical decrease of the shape parameter β from intrinsic breakdown (caused by electrical stress induced defect generation) to extrinsic breakdown (caused by defects induced by the manufacturing process).

Two different trap mechanisms, with decreased shape parameter β and increased scale parameter η, were observed under positive substrate biases. The statistical parameters of progressive breakdown were collected, which indicate that the creation of a percolation path of GaN power devices under substrate biases strongly depends on dielectric material itself, while the trap generation process relates to GaN buffer traps induced from deep-level traps.

Examining Overvoltage Ruggedness of P-Gate GaN HEMTs

The definition of essential ruggedness of power devices is the capability to safely withstand any surge energy. The surge ruggedness of the GaN HEMT, which has no or minimal avalanche capability, hasn't been fully understood to date. To help better comprehend it, thorough physics were applied to the surge-energy withstand process and the failure mechanisms of p-gate GaN HEMTs.[12]

With the qualification of GaN power HEMTs, we must consider the device ruggedness against any out-of-SOA (safe operating area) events. The key factor in power-device robustness is the ability to safely withstand surge energy. This capability is needed in many power applications, which include automotive systems, power grids, and more.

A widely used method to characterize a device's surge-energy capability is the unclamped inductive switching (UIS) *(Fig. 2)*.

The surge-energy withstand capability of GaN HEMTs isn't fully clear, mostly because the GaN HEMT is a power device that has no, or extraordinarily little, avalanche capability. This differs from Si and SiC MOSFETs, because no inherent p-n junctions are connected between the source and drain in GaN HEMTs.

Therefore, the holes generated during impact ionization and multiplication can't be effectively extracted. This limits the device's capability to accommodate the high current from unclamped inductive loads at high V_{ds}. The lack of avalanche capability might suggest a different surge-energy withstand dynamic within GaN HEMTs.

Surge-Energy Withstand Process

Reference 11 unveils the withstand process and failure mechanisms of commercial p-gate GaN HEMTs, which are under transient surge energy and overvoltage. It's implemented by a traditional UIS test coupled with a clamped inductive switching circuit that has a controlled parasitic inductance.

The surge-energy withstand process and failure mechanisms of GaN HEMTs are radically different from the Si and SiC MOSFETs with their avalanche capability. The GaN HEMT can withstand surge energy through its intrinsic overvoltage ability. However, it's not able to dissipate the surge energy during the withstand process.

The device failure, under surge energy, is mostly related to the peak overvoltage, but it isn't sensitive to dV/dt or duration of the surge voltage. The magnitude of surge energy is no longer a parameter that can directly reflect the device's intrinsic surge ruggedness for GaN HEMTs. The main failure mechanism is partly E-field limited and the breakdown locations in the device will be consistent with the peak E-field locations.

References

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