Electronic Design

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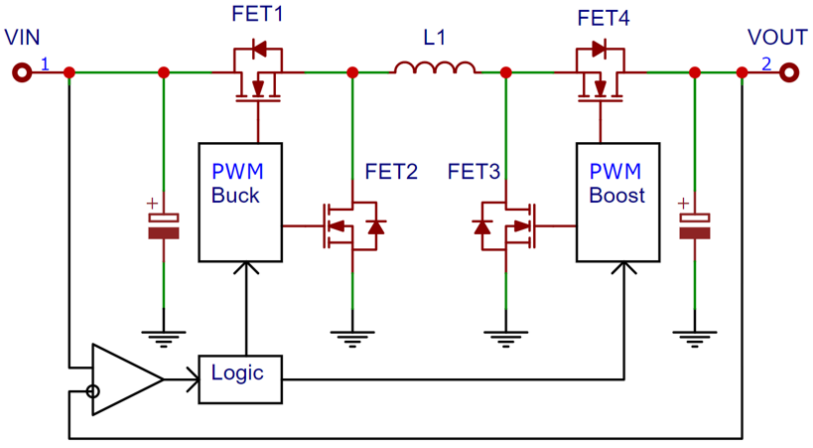
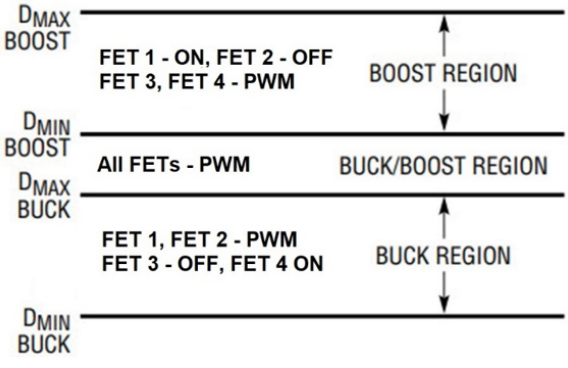
DC-DC Converter Design Basics (Part 3): Buck-Boost Converters

The final part of this series details how to build a buck-boost converter using the Renesas SLG47105.

DC-DC converters are widely used to efficiently produce a regulated voltage from a source that may or may not be well controlled to a load that may or may not be constant. This article series shows how DC-DC converters can be built using the Renesas SLG47105.



1. This buck-boost converter combines both (buck and boost) topologies.



2. This diagram shows the transition between modes depending on the input voltage.

Buck-Boost Converter

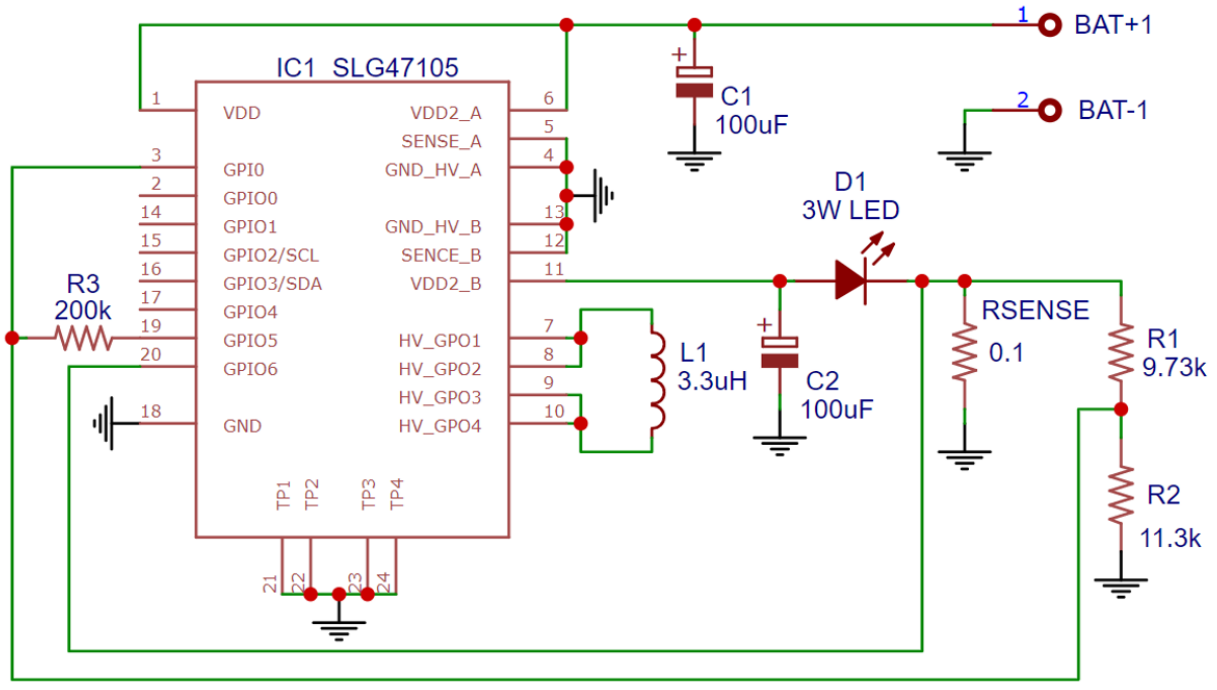
A buck-boost converter is a type of switched-mode power supply that combines the principles of the buck converter and the boost converter in a single circuit.

However, in many applications, such as battery-powered systems, the input voltage can vary widely, starting at full charge and gradually decreasing as the battery charge is used up. At full charge, where the battery voltage may be higher than needed by the circuit being powered, a buck regulator would be ideal to keep the supply voltage steady. But as the charge diminishes, the input voltage falls below the level required by the circuit, and either the battery must be discarded or recharged. At this point, the best alternative would be the boost regulator.

By combining these two regulator designs, it's possible to have a regulator circuit that can cope with a wide range of input voltages both higher and lower than that needed by the circuit. Fortunately, both buck and boost converters use very similar components; they just need to be rearranged, depending on the level of the input voltage.

In *Figure 1*, the common components of the buck and boost circuits are combined. A control unit is added, which senses the level of input voltage and then selects the appropriate circuit action.

This topology offers a simple solution with an approach



3. The buck-boost converter maintains a constant load current regardless of whether the input voltage is higher or lower than the output.

that requires neither cumbersome magnetics nor additional control loops. The design takes the form of a synchronous buck or boost, depending on the input voltage. Transitions between modes depend on the duty cycle and are quick and automatic *(Fig. 2)*.

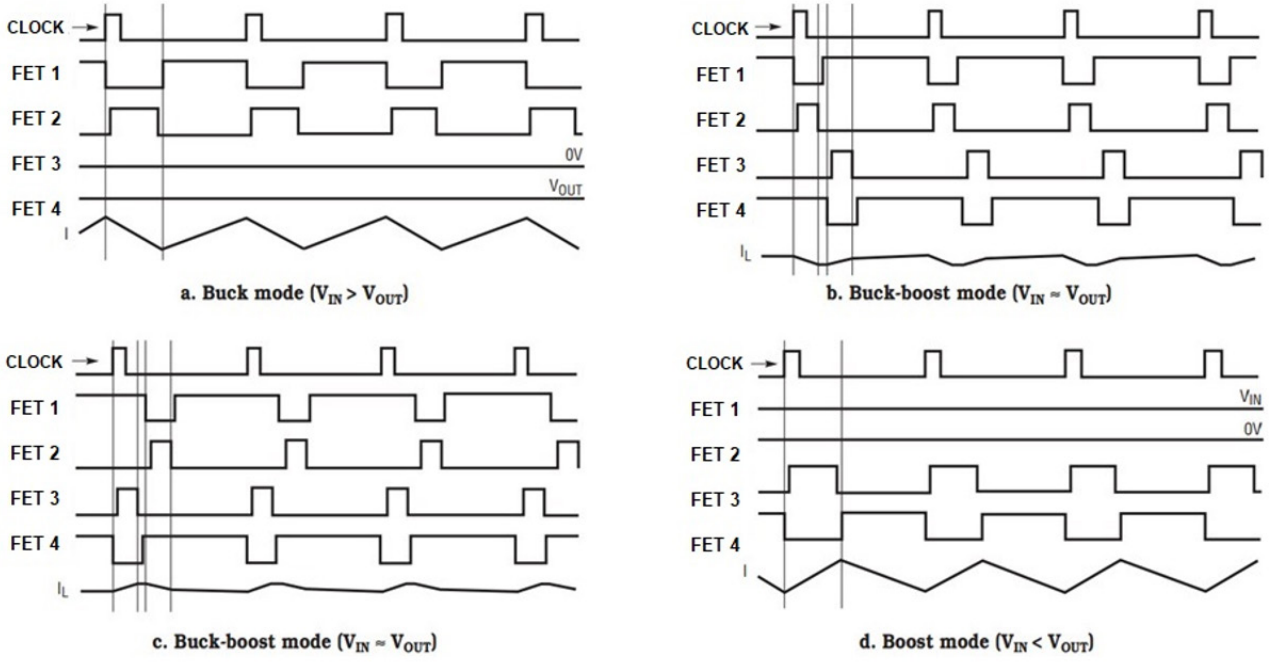
Example #1.: Powering LED from Single Li-ion Cell

As an example, a simple buck-boost converter was designed using the SLG47105 IC and Go Configure software *(Figs. 3 through 5)*. Its purpose is to drive a 3-W LED from a single Li-ion cell. It has the following parameters:

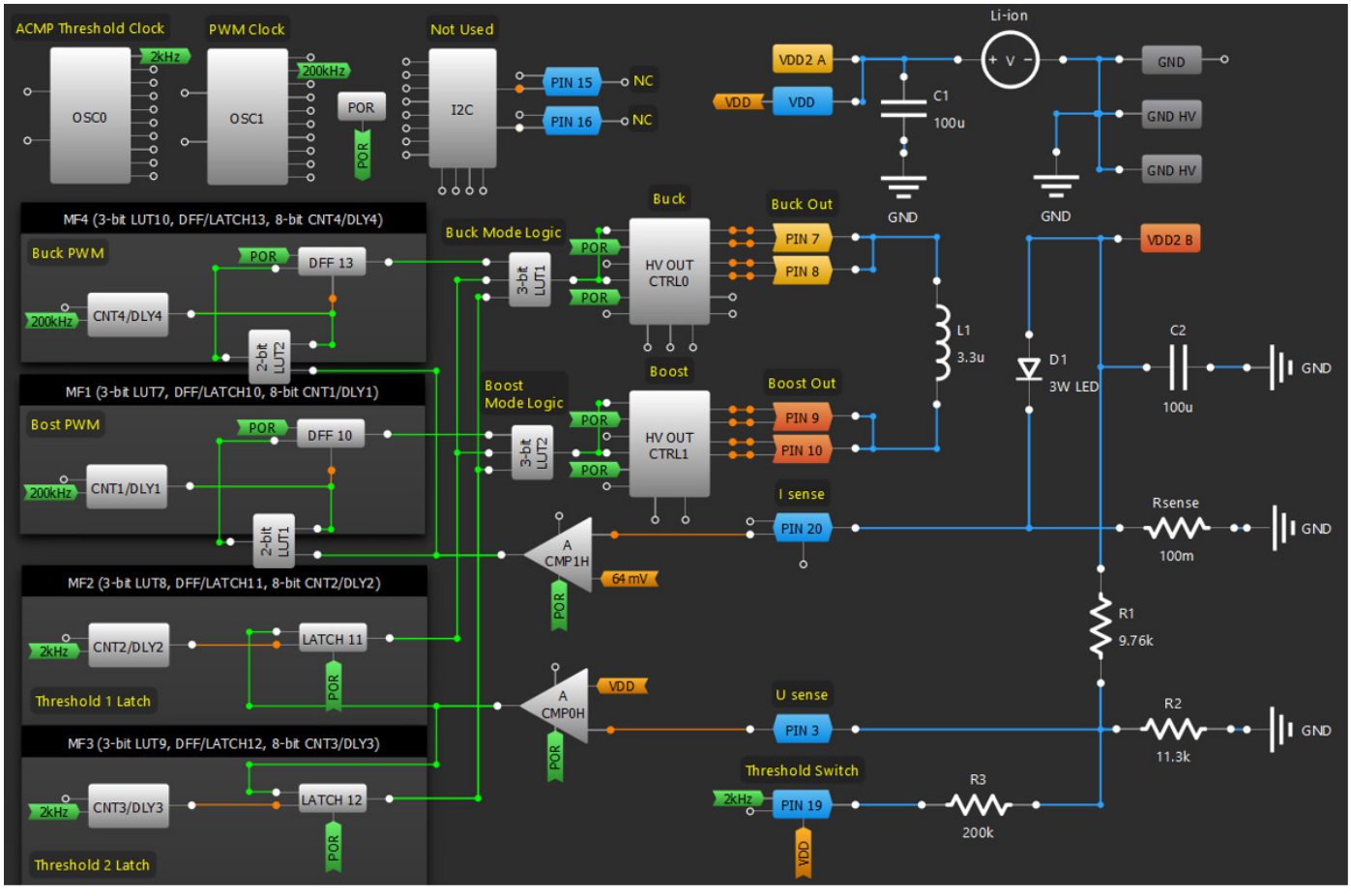
- Input voltage range: (V_{IN}) 2.7 V to 4.2 V
- Output voltage: 2.9 to 3.6 V (depending on the LED type)
- Output current range: 650 mA (regulated)
- PWM frequency: 200 kHz
- Overcurrent/short-circuit protection: Internal OCP

Calculated values for buck:

- Rated peak withstand current (I_{PK}): 1.3 A
- Inductance (L_{MIN}): 2 µH



4. This diagram shows the power-switch modes, depending on the input-voltage level, for Example #1.



5. This is Example #1 of the CC buck-boost DC-DC converter designed in the Go Configure software.

- Filter capacitor (C): 22 µF

Calculated values for boost:

- Min. duty cycle: 10%
- Max. duty cycle: 25%
- Min. inductor size: 1.9 µH
- Peak inductor current: 1.73 A
- Filter capacitor (C): 63 µF

Selected value of the inductance is 3.3 µH and for the filter capacitor it's 100 µF. *Figure 3* shows a schematic diagram.

Theory of Operation

Buck Mode

When the input is well above the output (buck mode), the converter behaves as in section 1.

Boost Mode

When the input is well below the output (boost mode), the converter behaves as in section 2.

Buck-Boost Mode

Ideally, the buck-boost mode is activated when the boost duty cycle passes its minimum and before buck mode starts. In practice, that causes a slight output voltage instability when transitioning from mode to mode. To avoid that, the buck-boost mode in this design has a bit wider active area at the cost of lower efficiency.

Figure 4 shows all modes for all four switches (FETs).

Go Configure Project

Both buck and boost regulators within this project are built using the same principles and macrocells as in previous buck and boost converters *(Fig. 5)*.

The buck PWM logic is built on MF4 (CNT4/DLY4 and DFF 13) and 2-bit LUT2. The CNT4/DLY4 sets the maximum duty cycle of 96.6 %. It remains at maximum until the feedback signal from the ACMP1H through 2-bit LUT2 cuts it. Thus, regulating the output voltage on the current sense resistor regulates the load current.

The boost PWM logic is built on MF1 (CNT1/DLY1 and DFF 10) and 2-bit LUT1. The CNT1/DLY1 sets the minimum duty cycle of 10 %. It remains at a minimum until the feedback signal from the ACMP1H through 2-bit LUT1 extends it to the width when the voltage on the current-sense resistor is equal to the Vref maintaining a constant load current.

Both HV OUT macrocells are configured as fast slew-rate half-bridge output. Each macrocell has two half-bridge outputs that are connected in parallel to handle higher output current. All four HV pins (Pin 7 to Pin 9) are configured to «High and Low side on».

The ACMP1H in this design is used in a voltage-feedback

loop so that both PWMs could stabilize the current-sensor voltage, thus maintaining constant current on the load. The output current is determined by the ACMP's Vref and the current-sensor resistance. For the 3-W LED used in this project, the output current should be around 700 mA at a voltage of about 3.6 V. If the current-sense resistor value is 0.1 Ω, than:

$$Vref = 700mA \times 0.1\,\Omega = 700\,mV$$

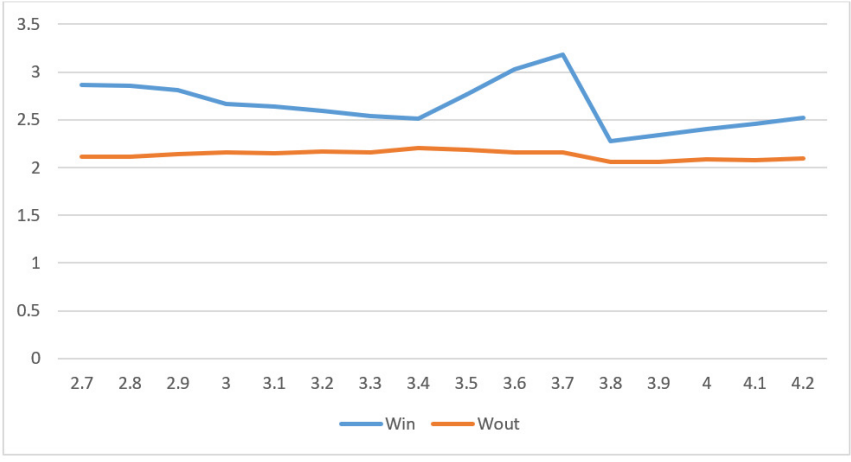
The closest Vref value available in the SLG47105 is 64 mV, which is close enough. The output current can be adjusted by changing the current-sense resistor value if needed.

The ACMP0H serves as a cross-voltage detector. Its positive input is connected internally to the VDD (VDD and VDDA are connected together) through the 1/2 internal voltage divider. The negative input is connected to the output through the voltage divider R1R2, too. However, this one is modified by adding one more resistor R3, which periodically (with 2-kHz frequency) is being connected in parallel to the R2 through open drain PIN 19, making two thresholds for ACMP0H.

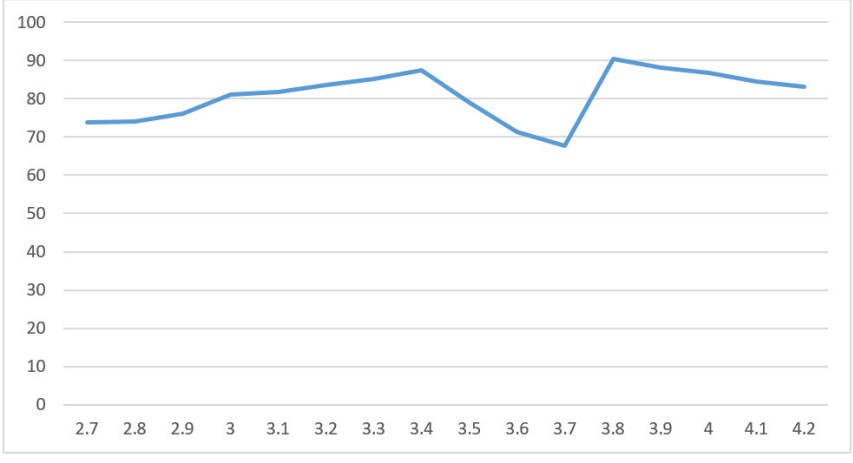
At the same time, the clock frequency of 2 kHz (from OSC0) goes to two edge detectors within MF2 and MF3 (rising and falling respectively). Together with latches 11 and 12, they latch ACMP's output for each threshold. This circuit (ACMP0H, OSC0, PIN 19, MF2, and MF3) enables detecting when the input voltage is close to the output voltage with two thresholds—$V_{IN} < V_{OUT}$ and $V_{IN} > V_{OUT}$—creating a window for the buck-boost mode.

3-bit LUTs 1 and 2 make a logic that's based on the signals from the previously described circuit, which turns on and off the respective mode: buck, boost, or buck-boost. The graphs in *Figures 6 and 7* show the device's performance.

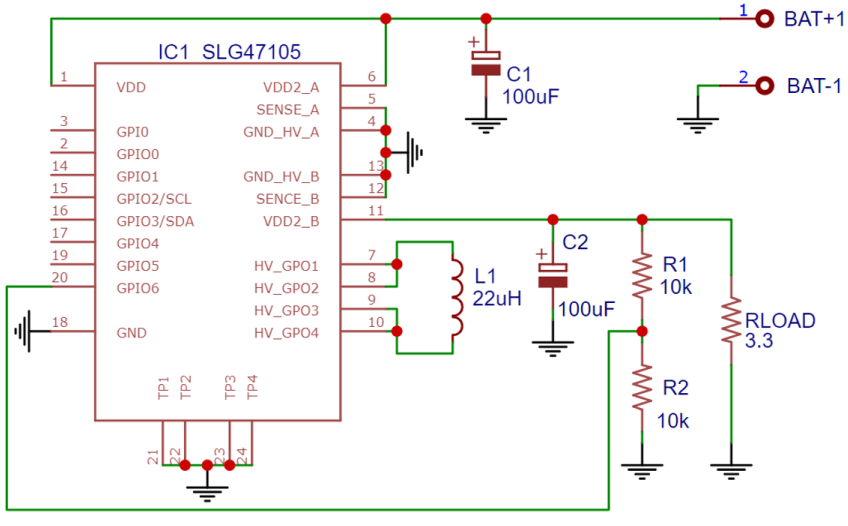
8. The buck-boost converter maintains a constant load voltage regardless of whether the input voltage is higher or lower than the output.

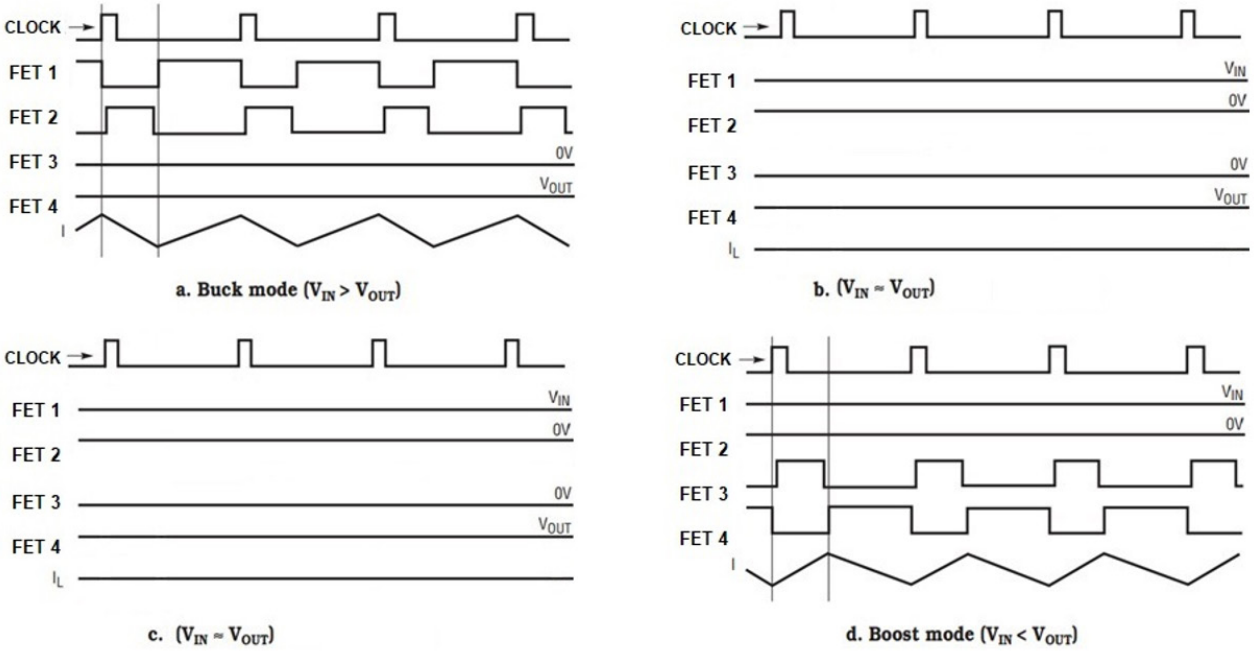


6. This graph shows input and output power versus input voltage for Example #1.

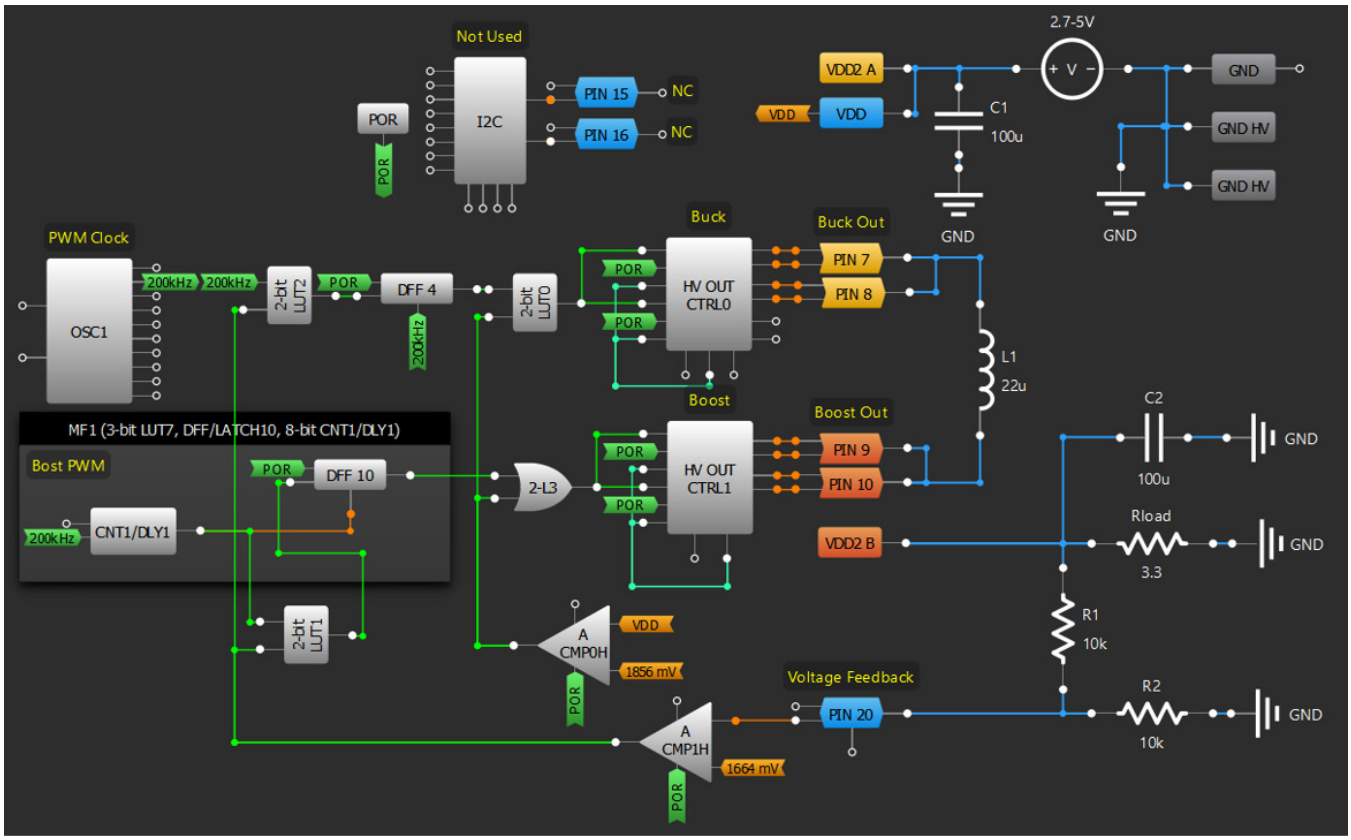


7. This graph illustrates efficiency versus input voltage for Example #1.

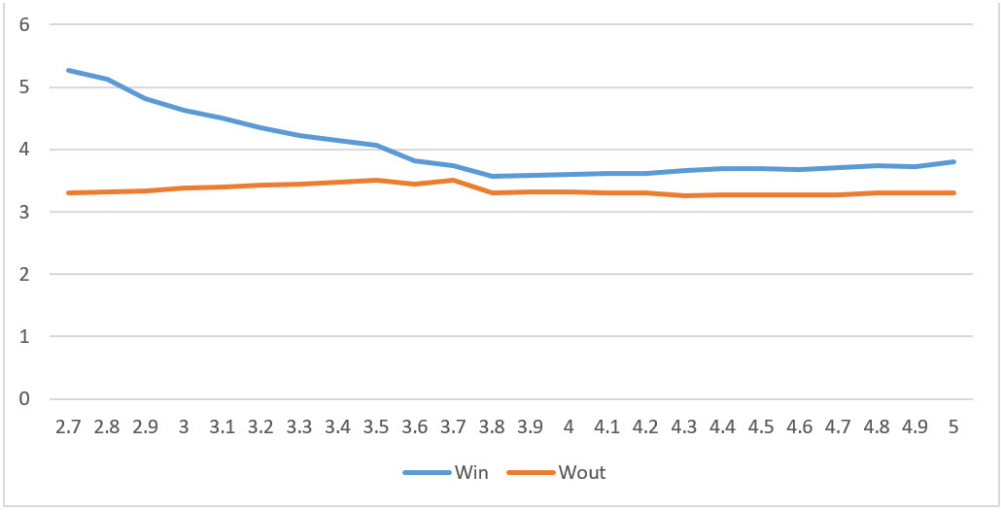




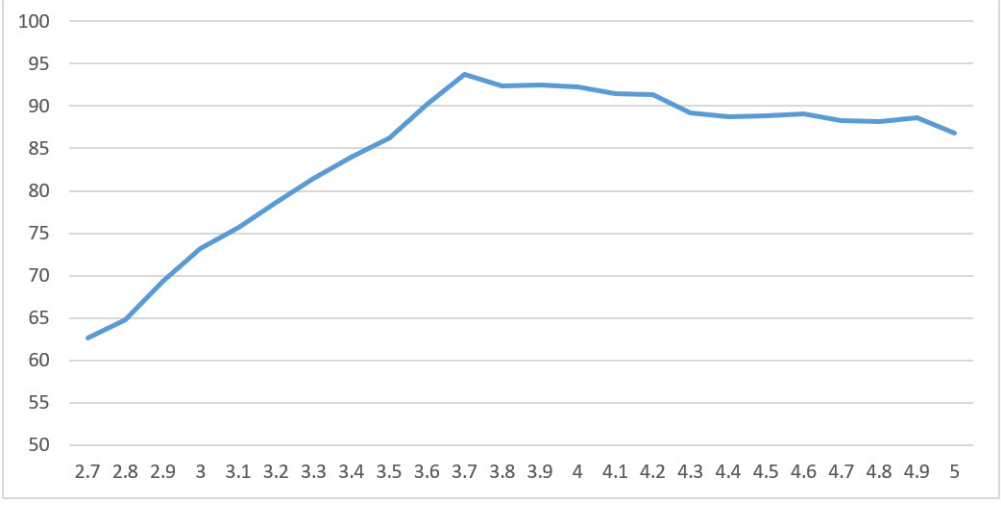
9. This diagram shows the power-switch modes depending on the input-voltage level for Example #2.



10. This is Example #2 of the CV buck-boost DC-DC converter designed in the Go Configure software.



11. This graph shows input and output power versus input voltage for Example #2.



12. This graph shows efficiency versus input voltage for Example #2.

Example #2: 3.3-V Output from 2.7- to 5.0-V Input

This buck-boost converter is very similar to the previous one, but uses a non-standard approach to switch between modes. When V_{IN} approaches V_{OUT} (taking into account internal switches' voltage drop) instead of engaging both buck and boost modes, this converter does exactly the opposite. Both modes are being disabled, enabling V_{IN} to go through the output pins straight to the load uninterrupted by any PWM. As a result, the efficiency gap can be eliminated at the cost of a slight V_{OUT} wobble in the transition moment *(Fig. 8)*.

The goal is to get a stable 3.3-V, 1-A supply from the 2.7- to 5.0-V input-voltage range. It has the following parameters:

- Input-voltage range (V_{IN}): 2.7 to 5 V
- Output voltage (V_{OUT}): 3.3 V (regulated)
- Output current range: 1 A
- PWM frequency: 200 kHz
- Overcurrent/short-circuit protection: Internal OCP

Theory of Operation

The buck and boost modes work the same way as described in the previous example. However, there's no buck-boost mode. As mentioned, instead of engaging two modes simultaneously, the input voltage is routed through the internal switches directly to the load *(Fig. 9)*.

Go Configure Project

Both buck and boost regulators within this project are built using the same principles as in the previous buck-boost converter *(Fig. 10)*.

The buck PWM logic is built on 2-bit LUT2 and DFF 4. The maximum duty cycle of 99 % is achieved by omitting the delay and using the clock signal directly from the flexible divider. It remains at maximum until the feedback signal from the ACMP1H through 2-bit LUT2 cuts it, thus regulating the output voltage.

The boost PWM logic is built on MF1 (CNT1/DLY1

and DFF 10) and 2-bit LUT1. The CNT1/DLY1 sets the minimum duty cycle of 25%. It remains at a minimum until the feedback signal from the ACMP1H through 2-bit LUT1 extends it to the width when the output voltage is twice the Vref maintaining a constant V_{OUT}.

Both HV OUT macrocells are configured as fast slew-rate half-bridge output. Each macrocell has two half-bridge outputs that are connected in parallel to handle higher output current. All four HV pins (Pin 7 to Pin 9) are configured to «High and Low side on».

The ACMP1H in this design is used in a voltage-feedback loop so that both PWMs could stabilize the output voltage. The output voltage is determined by the ACMP's Vref and the R1R2 voltage divider. In this case:

$$\boldsymbol{Vout = Vref \times \left(\frac{R1}{R2} + 1\right) = 1664\,mV \times \left(\frac{10k}{10k} + 1\right) = 3.328\,V}$$

The ACMP0H serves as a cross-voltage detector. Its positive input is connected internally to the VDD (VDD and VDDA are connected together) through the 1/2 internal voltage divider, which is compared to the internal Vref of 1,856 mV with an internal 32-mV hysteresis.

That's chosen higher to compensate for the internal transistors' voltage drop under the load. It should be noted that the value of 1856 mV is selected for 1-A load. If the output current is different, this value should be adjusted. But if the load is planned to be variable, in this case, instead of an internal Vref, the external voltage divider (with a 1/2 ratio) should be used. It must be connected between Vout, Pin 3, (ACMP0H IN-), and GND.

Also, to avoid ACMP oscillation, external hysteresis must be considered (in this case, internal 32-mV hysteresis will be unavailable). To do that, the ACMP0H output must be connected to any available output pin, and from that pin, a 200-kΩ resistor should be connected to Pin 3 (ACMP0H IN-).

The graphs in *Figures 11 and 12* show the device's performance.

Conclusions

Optional section, remove if not required. This section contains any conclusions based on the content of the document.

As can be seen, designing and building buck-boost converters using the HVPAK SLG47105 chip is quite easy. The amount of unused macrocells leaves plenty of room for modifications and adding new features for proposed designs.

For example, a soft-start where a PWM period slowly increases from 0 to the required value reduces a peak startup current, programmable overcurrent protection, multiple output voltages, etc. Also, the HV OUT pins are suitable for driving external MOSFETs, which allows for building a very high-power DC-DC converter.

Nazar Sliunchenko graduated from National University "Lviv Polytechnic" in 2008, studying at the Department of Telecommunications, Radioelectronics & Electronic Engineering. He has more than 15 years of experience in hardware design, including analog and digital devices. Currently, Nazar is managing one of the Technical Documentation departments at Renesas Electronics Corp.

References

Go Configure Software

GP file https://www.renesas.com/document/scd/cm-358-gp-file

Buck-Boost Converters

Breakthrough Buck-Boost Controller

https://x-engineer.org/dc-dc-converter/