6U OpenVPX 9-Slot BKP6-CEN09-11.2.13-n Backplane

*Photo shown is of 6U, 5-slot backplane.

Description

The Elma Bustronic BKP6-CEN09-11.2.13-1 6U OpenVPX backplane comes in a Star central slot topology with fat pipes routed to each slot.

Features

- Compliant to ANSI/VITA 65-2010
- Compliant to the latest VITA 46 Specifications
- High-speed Multi-gig connector
- Rugged Eurocard form factor in 6U height
- Provides built in ESD ground protection in every slot
- Signal integrity analysis report available upon request

Board Specifications

- Layers TBD
- 2 oz. power and ground
- PCB FR-4 or equivalent
- PCB thickness TBD

Mechanical Specifications

- 6U height
- 9 slots
- MultiGig RT-2 connectors

Close-up of Multi-Gig connector

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Line Drawing

Coming Soon!

Order Information

Height	Total Slots	Description	Profile Number	Part Number
6U	9	VPX central switch, up to 3.125 Gbps per channel	BKP6-CEN09-11.2.13-1	1OVX609VX1-1X01R
6U	5	VPX central switch, up to 3.125 Gbps, no RTM connectors	BKP6-CEN09-11.2.13-1	1OVX609VX1-1X00R

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J0 Signal Assignments

	Row I	Row H	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	Vs1	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2	Vs2
2	Vs1	Vs1	Vs1	Vs1	No Pad	Vs2	Vs2	Vs2	Vs2
3	Vs3	Vs3	Vs3	Vs3	No Pad	Vs3	Vs3	Vs3	Vs3
4	GND	SM2	SM3	GND	-12V_Aux	GND	SYSRESET*	NVMRO	GND
5	GND	GAP*	GA4*	GND	3.3V_Aux	GND	SM0	SM1	GND
6	GND	GA3*	GA2*	GND	+12V_Aux	GND	GA1*	GA0*	GND
7	TCK	GND	GND	TDO	TDI	GND	GND	TMS	TRST*
8	GND	REF_CLK-	REF_CLK+	GND	GND	AUX_CLK-	AUX_CLK+	GND	GND

J1/P1 Payload Slot Signal Assignments

Plug-In Module P1		Row G	Row F	Row E		Row D	Row C	Row B		Row A
				Even	Odd			Even	Odd	
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1	GDiscrete1	GND	GND-J1	DP01-T0-	DP01-T0+	GND	GND-J1	DP01-R0-	DP01-R0+
2		GND	DP01-T1-	DP01-T1+	GND-J1	GND	DP01-R1-	DP01-R1+	GND-J1	GND
3		P1-VBAT	GND	GND-J1	DP01-T2-	DP01-T2+	GND	GND-J1	DP01-R2-	DP01-R2+
4		GND	DP01-T3-	DP01-T3+	GND-J1	GND	DP01-R3-	DP01-R3+	GND-J1	GND
5	Data Plane Port 2	SYS_CON*	GND	GND-J1	DP02-T0-	DP02-T0+	GND	GND-J1	DP02-R0-	DP02-R0+
6		GND	DP02-T1-	DP02-T1+	GND-J1	GND	DP02-R1-	DP02-R1+	GND-J1	GND
7		Reserved	GND	GND-J1	DP02-T2-	DP02-T2+	GND	GND-J1	DP02-R2-	DP02-R2+
8		GND	DP02-T3-	DP02-T3+	GND-J1	GND	DP02-R3-	DP02-R3+	GND-J1	GND
9	Data Plane Port 3	UD	GND	GND-J1	DP03-T0-	DP03-T0+	GND	GND-J1	DP03-R0-	DP03-R0+
10		GND	DP03-T1-	DP03-T1+	GND-J1	GND	DP03-R1-	DP03-R1+	GND-J1	GND
11		UD	GND	GND-J1	DP03-T2-	DP03-T2+	GND	GND-J1	DP03-R2-	DP03-R2+
12		GND	DP03-T3-	DP03-T3+	GND-J1	GND	DP03-R3-	DP03-R3+	GND-J1	GND
13	Data Plane Port 4	UD	GND	GND-J1	DP04-T0-	DP04-T0+	GND	GND-J1	DP04-R0-	DP04-R0+
14		GND	DP04-T1-	DP04-T1+	GND-J1	GND	DP04-R1-	DP04-R1+	GND-J1	GND
15		Maskable Reset*	GND	GND-J1	DP04-T2-	DP04-T2+	GND	GND-J1	DP04-R2-	DP04-R2+
16		GND	DP04-T3-	DP04-T3+	GND-J1	GND	DP04-R3-	DP04-R3+	GND-J1	GND

J2/P2 Payload Slot Signal Assignments

Plug-In Module P2		Row G	Row F	Row E		Row D	Row C	Row B		Row A
				Even	Odd			Even	Odd	
Bplane J2		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 5	UD	GND	GND-J2	DP05-T0-	DP05-T0+	GND	GND-J2	DP05-R0-	DP05-R0+
2		GND	DP05-T1-	DP05-T1+	GND-J2	GND	DP05-R1-	DP05-R1+	GND-J2	GND
3		UD	GND	GND-J2	DP05-T2-	DP05-T2+	GND	GND-J2	DP05-R2-	DP05-R2+
4		GND	DP05-T3-	DP05-T3+	GND-J2	GND	DP05-R3-	DP05-R3+	GND-J2	GND
5	Data Plane Port 6	UD	GND	GND-J2	DP06-T0-	DP06-T0+	GND	GND-J2	DP06-R0-	DP06-R0+
6		GND	DP06-T1-	DP06-T1+	GND-J2	GND	DP06-R1-	DP06-R1+	GND-J2	GND
7		UD	GND	GND-J2	DP06-T2-	DP06-T2+	GND	GND-J2	DP06-R2-	DP06-R2+
8		GND	DP06-T3-	DP06-T3+	GND-J2	GND	DP06-R3-	DP06-R3+	GND-J2	GND
9	Data Plane Port 7	UD	GND	GND-J2	DP07-T0-	DP07-T0+	GND	GND-J2	DP07-R0-	DP07-R0+
10		GND	DP07-T1-	DP07-T1+	GND-J2	GND	DP07-R1-	DP07-R1+	GND-J2	GND
11		UD	GND	GND-J2	DP07-T2-	DP07-T2+	GND	GND-J2	DP07-R2-	DP07-R2+
12		GND	DP07-T3-	DP07-T3+	GND-J2	GND	DP07-R3-	DP07-R3+	GND-J2	GND
13	Data Plane Port 8	UD	GND	GND-J2	DP08-T0-	DP08-T0+	GND	GND-J2	DP08-R0-	DP08-R0+
14		GND	DP08-T1-	DP08-T1+	GND-J2	GND	DP08-R1-	DP08-R1+	GND-J2	GND
15		UD	GND	GND-J2	DP08-T2-	DP08-T2+	GND	GND-J2	DP08-R2-	DP08-R2+
16		GND	DP08-T3-	DP08-T3+	GND-J2	GND	DP08-R3-	DP08-R3+	GND-J2	GND

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J4/P4 Payload Slot Signal Assignments

Plug-In Mod P4		Row G	Row F	Row E		Row D	Row C	Row B		Row A
				Even	Odd			Even	Odd	
Bplane J4		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	User Defined	UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
2		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
3		UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
4		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
5		UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
6		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
7		UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
8		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
9		UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
10		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
11	RSVD	UD	GND	GND-J4	RSVD	RSVD	GND	GND-J4	RSVD	RSVD
12		GND	RSVD	RSVD	GND-J4	GND	RSVD	RSVD	GND-J4	GND
13	User Defined	UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
14		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
15		UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
16		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND

J3, J5-J6 Payload Slot Signal Assignments = User Defined

J1/P1 Switch Slot Signal Assignments

Plug-In Module P1		Row G	Row F	Row E		Row D	Row C	Row B		Row A
				Even	Odd			Even	Odd	
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1	GDiscrete1	GND	GND-J1	DP01-T0-	DP01-T0+	GND	GND-J1	DP01-R0-	DP01-R0+
2		GND	DP01-T1-	DP01-T1+	GND-J1	GND	DP01-R1-	DP01-R1+	GND-J1	GND
3		P1-VBAT	GND	GND-J1	DP01-T2-	DP01-T2+	GND	GND-J1	DP01-R2-	DP01-R2+
4		GND	DP01-T3-	DP01-T3+	GND-J1	GND	DP01-R3-	DP01-R3+	GND-J1	GND
5	Data Plane Port 2	SYS_CON*	GND	GND-J1	DP02-T0-	DP02-T0+	GND	GND-J1	DP02-R0-	DP02-R0+
6		GND	DP02-T1-	DP02-T1+	GND-J1	GND	DP02-R1-	DP02-R1+	GND-J1	GND
7		Reserved	GND	GND-J1	DP02-T2-	DP02-T2+	GND	GND-J1	DP02-R2-	DP02-R2+
8		GND	DP02-T3-	DP02-T3+	GND-J1	GND	DP02-R3-	DP02-R3+	GND-J1	GND
9	User Defined	UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
10		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
11		UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
12		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
13		UD	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
14		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND
15		Maskable Reset*	GND	GND-J1	UD	UD	GND	GND-J1	UD	UD
16		GND	UD	UD	GND-J1	GND	UD	UD	GND-J1	GND

J2-J6 Payload Slot Signal Assignments = User Defined

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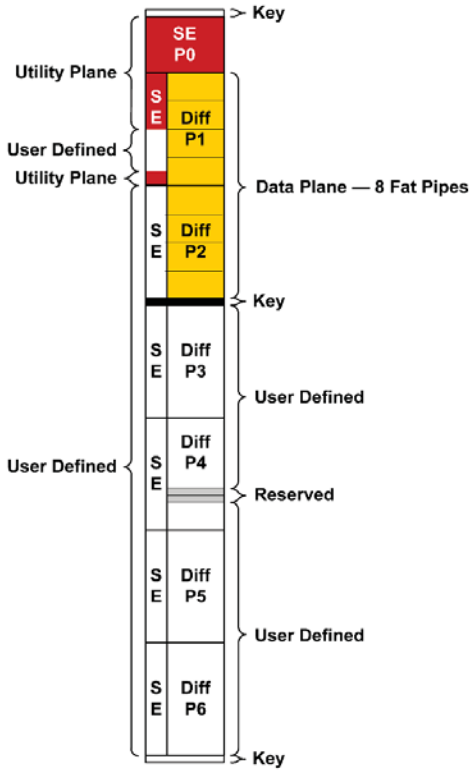
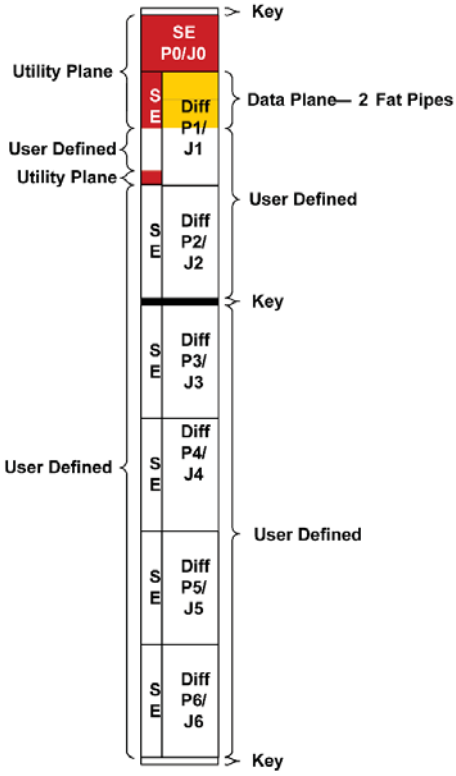
Payload Slot Profile



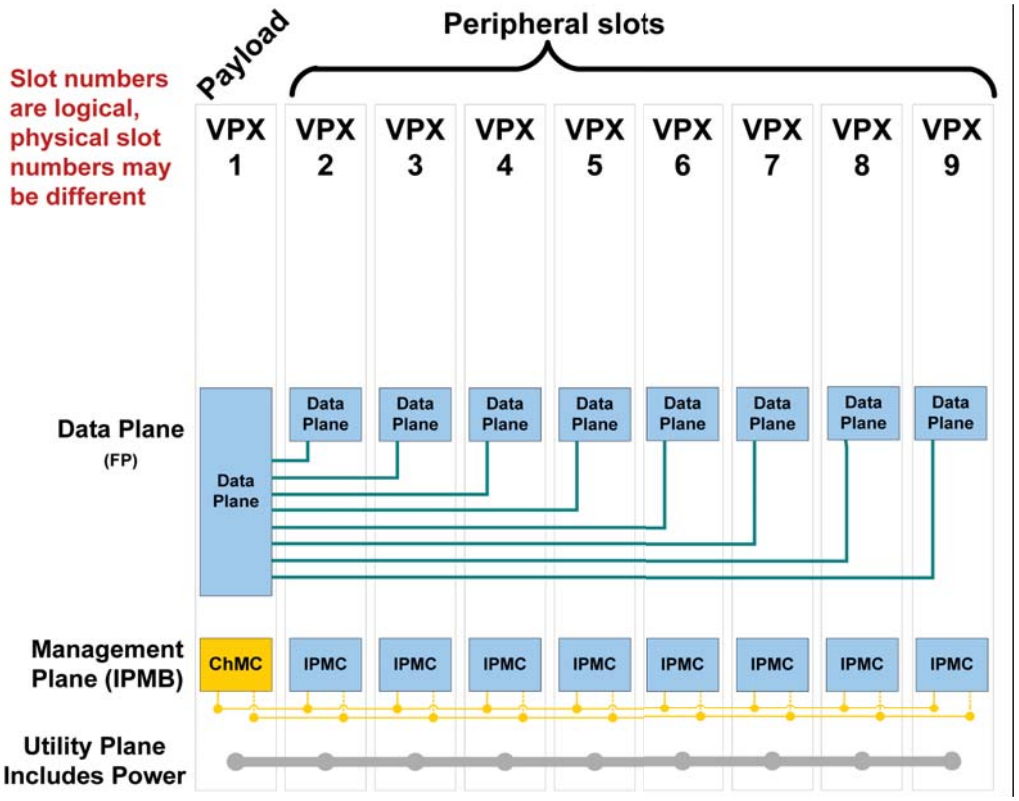
SLT6-PAY-8F-10.2.3

Peripheral Slot Profile



SLT6-PER-2F-10.3.2

Backplane Topology



6U OpenVPX 9-Slot BKP6-CEN09-11.2.13-n Backplane

Backplane Profile

	Mechanical		Slot Profiles and Section		Channel Gbaud Rate
			VPX 1	VPX 2 - 9	
Profile name	Pitch (in)	RTM Conn	Payload	Payload or Peripheral	Data Plane
BKP6-CEN06-11.2.13-1	1.0	VITA 46.10	SLT6-PAY-8F-10.2.3	SLT6-PER-2F-10.3.2	2.5
BKP6-CEN06-11.2.13-2	1.0	VITA 46.10	SLT6-PAY-8F-10.2.3	SLT6-PER-2F-10.3.2	5.0
BKP6-CEN06-11.2.13-3	1.0	VITA 46.10	SLT6-PAY-8F-10.2.3	SLT6-PER-2F-10.3.2	6.25

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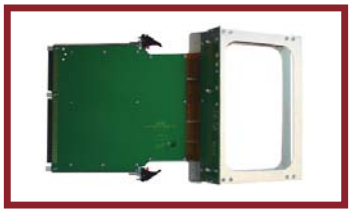

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