

Flat-Panel Phased-Array Antenna Design

Though they're poised to take off, limitations in available chipsets have held flat-panel phased arrays back. With advances in GaN-process and IC-packaging technologies, the benefits of these arrays are becoming too alluring to resist.

Advances in semiconductor technology have enabled the proliferation of phased-array antennas across the industry. This shift away from mechanically steered antennas to active electronically scanned antennas (AESAs) began years ago in military applications, but of late it's rapidly advanced in satcom-on-the-move and 5G communications.

The low-profile AESA has advantages such as fast steering capability, the ability to produce multiple radiation patterns, and higher reliability. However, these antennas required significant advances in IC technology before they could become widely available. Planar phased arrays require devices operating with high levels of integration, low power consumption, and high efficiency so that users may fit these components behind the antenna array while keeping heat generation to acceptable levels.

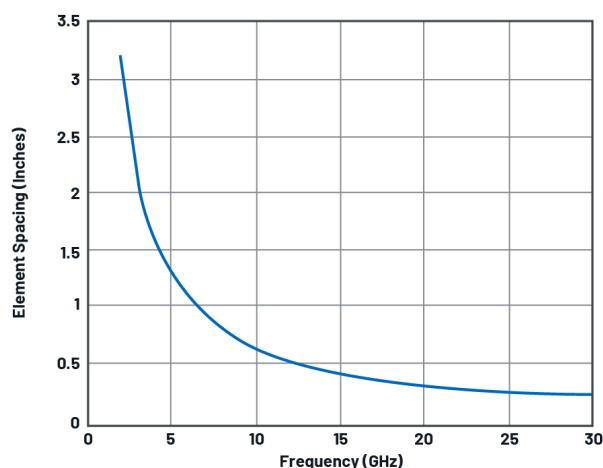
This article will briefly describe how advances in phased-array chipsets are making planar phased-array antennas possible, followed by examples.

THE ADVENT OF PHASED ARRAYS

In past years, parabolic dish antennas have been widely used to transmit and receive signals where directivity is important. Thanks to years of optimizations, many of those systems work well and are relatively low in cost. However, mechanically steered dish antennas do have some drawbacks. They're physically large, slow to steer, have worse long-term reliability, and provide just one desired radiation pattern or data stream.

Phased-array antennas are electrically steered and offer numerous benefits such as having a lower profile, less volume, improved long-term reliability, faster steering, and multiple beams. A key aspect of the phased-array antenna design is the spacing of the antenna elements. The approximately half-wavelength element spacing needed for most arrays creates particularly challenging designs at higher frequencies.

Interest in using phased-array antenna technology for vari-

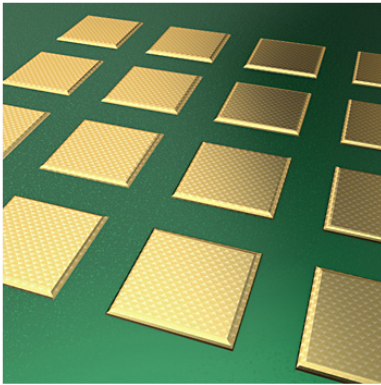


1. From this graph of maximum antenna-element spacing in inches vs. frequency, it's clear that with increasing frequency it becomes more difficult to fit components behind the antenna.

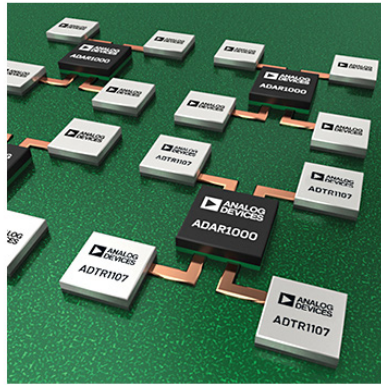
ous applications has been strong. However, their feasibility is limited by the available ICs. With the recent developments in phased-array chipsets, this is no longer the case. Semiconductor technology is moving toward advanced silicon ICs that combine digital controls, memory, and RF transistors onto the same chip. Not only that, but gallium-nitride (GaN) process technology is significantly increasing the power density of power amplifiers, which results in a much smaller footprint.

TECHNOLOGY TABLES TURN

There's a major shift underway toward low-profile arrays that consume less volume and weight. The traditional plank architecture essentially uses small printed-circuit-board (PCB) planks bearing circuitry that's perpendicularly fed into the back side of the antenna PCB. This approach has continually improved over 20 years to reduce the size of the plank, thereby reducing the depth of the antenna.



PCB Top



PCB Bottom

2. The image on the left shows the gold patch-antenna elements on the top side of the PCB; the image on the right shows the analog front end of the antenna on the bottom side of the PCB.

Next-generation designs move from the plank architecture to a flat-panel approach. Such designs substantially reduce the depth of antennas, making them easier to fit into portable or airborne applications. Achieving smaller size requires enough integration in each IC to fit them on the back side of the antenna.

In planar-array designs, the space available for ICs on the back side of the antenna is limited by the antenna-element spacing. For example, the maximum antenna-element spacing to prevent grating lobes for up to a 60-degree scan angle is 0.54λ . *Figure 1* shows this maximum element spacing in inches vs. frequency. At higher frequencies, the spacing between the elements becomes quite small, leaving little room for components behind the antenna.

In *Figure 2*, the image on the left shows the gold patch-antenna elements on the top side of the PCB, while the image on the right shows the analog front end of the antenna on the bottom side of the PCB. It's typical in such designs for a frequency-conversion stage and distribution network to reside on additional PCB layers.

It can easily be seen that more integrated ICs significantly diminish the challenges in laying out the antenna design with the required spacing. As the antenna shrinks with more electronics packed into a reduced footprint, it demands new semiconductor and packaging technology to help make the solutions viable.

SEMICONDUCTOR TECHNOLOGY AND PACKAGING

Figure 3 shows the microwave and millimeter-wave (mmWave) IC components used as building blocks for a phased-array antenna. In the beamforming IC

section, the attenuator adjusts the power level at each antenna element to reduce the sidelobes of the antenna pattern. The phase shifter adjusts the phase of each antenna element to steer the antenna's main beam, and a switch toggles between transmitter and receiver paths.

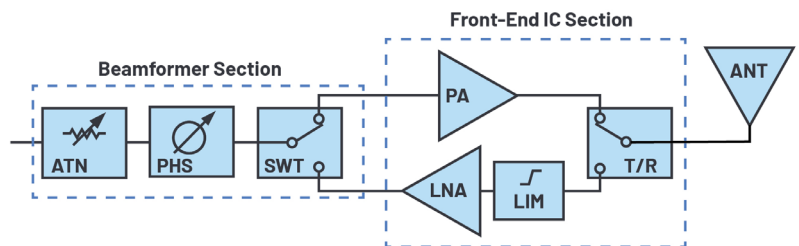
In the front-end IC section, a power amplifier (PA) boosts the transmit signal, a low-noise amplifier (LNA) improves the received signal, and, finally, a transmit/receive (T/R) switch toggles between the transmitter and receiver. In past implementations, the beamforming and front-end ICs were separately packaged devices. More advanced solutions might entail an integrated monolithic single-channel gallium-arsenide (GaAs) IC to achieve

this functionality. In addition, a passive RF combiner network, receiver/exciter, and signal processor (not shown) are included in most phased arrays in front of the beamformer.

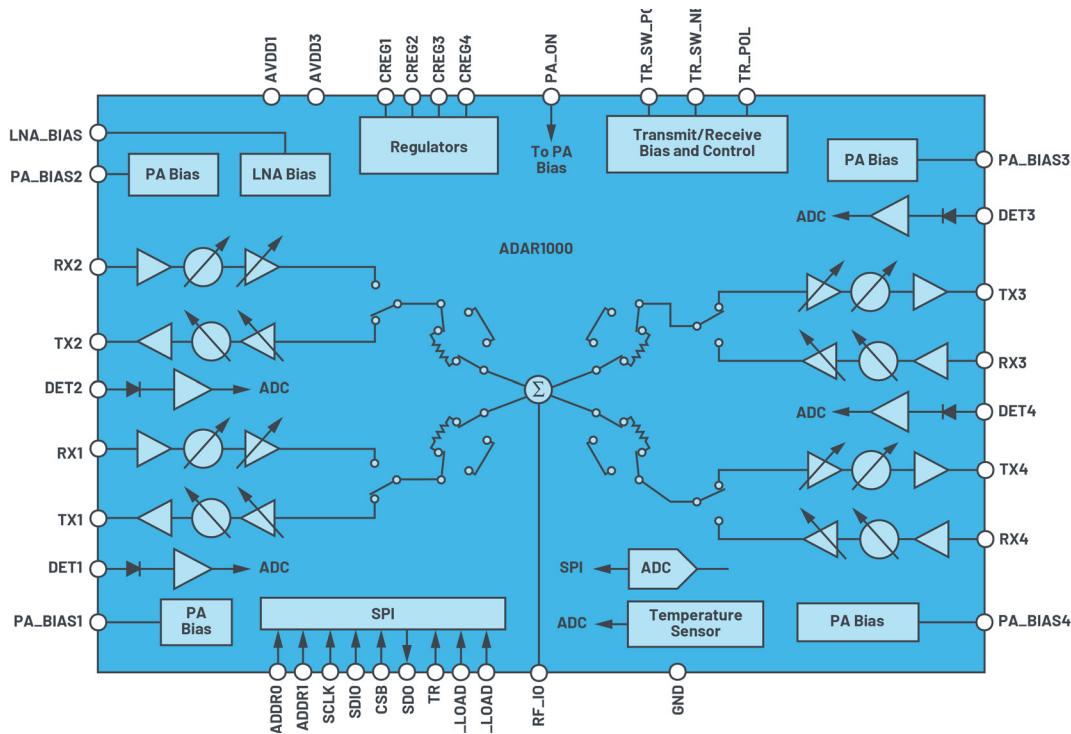
The recent proliferation of phased-array antenna technology has been aided by enhancements in semiconductor technology. The advanced nodes in silicon-germanium (SiGe) BiCMOS, silicon-on-insulator (SOI), and bulk CMOS have combined digital and RF circuitry. These ICs can perform the digital tasks in the array even as they control the RF signal path to achieve the desired phase and amplitude adjustment. It's possible today to achieve multichannel beamforming ICs for mmWave implementations that adjust gain and phase in configurations from four to as many as 32 channels.

In some lower-power scenarios, a silicon-based IC could be a monolithic solution for all of the previous functions. In high-power applications, GaN-based power amplifiers have significantly increased the power density that may be fit into the unit cell of a phased-array antenna. These amplifiers have traditional traveling-wave-tube (TWT)-based technology or relatively low-power GaAs-based ICs.

In airborne applications, we're seeing a trend to flat-panel architectures with the power-added efficiency (PAE) benefits of GaN technology. GaN has also enabled large ground-based



3. This simplified schematic depicts the microwave and mmWave ICs comprising a typical RF front end of a phased-array antenna.



4. This is a functional block diagram of the ADAR1000 X-/Ku-band beamforming IC, a four-channel device covering 8 to 16 GHz.

radars to move from a dish antenna, driven by a TWT, to phased-array-based antenna technology, driven by solid-state GaN ICs. We now have monolithic GaN ICs delivering over 100 W of power with over 50% PAE. Combining this level of efficiency with the low duty cycle of radar applications allows for surface-mount solutions in which it's possible to dissipate the heat generated through the package base. Such surface-mount PAs greatly reduce the size, weight, and cost of the antenna array.

On top of the pure power capabilities of GaN is the size reduction compared to existing GaAs IC solutions. As an example, a 6- to 8-W, GaN-based power amplifier at X-band reduces the footprint by 50% or more compared to a GaAs-based amplifier. That's important when you're trying to fit these electronics into the unit cell of a phased-array antenna.

Advances in packaging technology also dramatically lower the cost of planar antenna architectures. High-reliability designs may use gold-plated, hermetically sealed housings with chip-and-wire interconnects inside. While more robust for extreme environments, such housings are large and costly. Multichip modules (MCMs) combine multiple MMIC devices along with passive components within a relatively low-cost surface-mount package.

MCMs still allow for the mixing of semiconductor technologies so that the performance of each device can be maximized while saving considerable space. For example, in the case of a front-end IC, it may contain a PA, an LNA, and a T/R switch. Thermal vias, or the solid copper slug in the base of the package, conduct heat away from the circuitry. In the inter-

est of cost savings, commercial, military, and space applications are now using the significantly lower-cost surface-mount packaging alternatives in many applications.

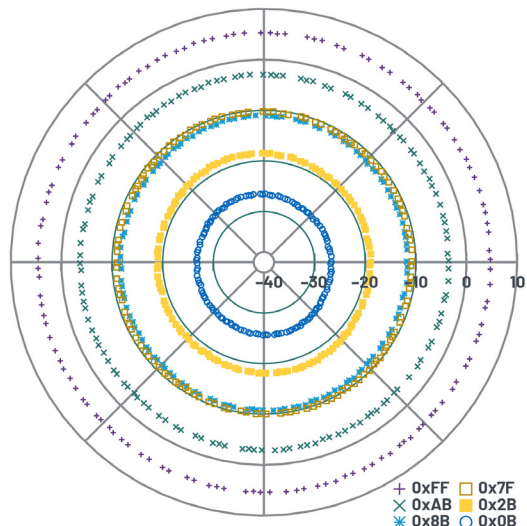
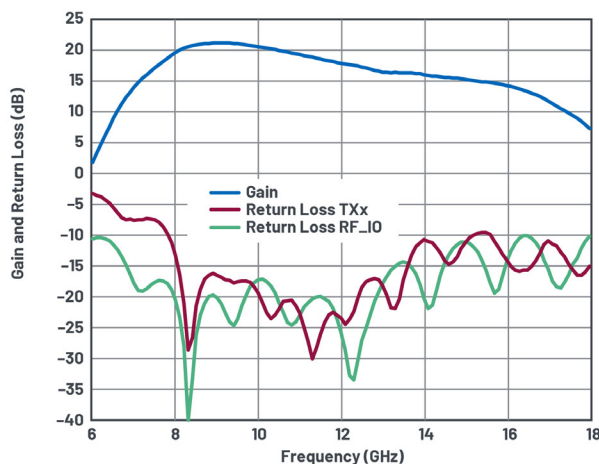
PHASED-ARRAY BEAMFORMER ICs

Integrated analog beamforming ICs, often called core chips, support a range of applications, including radar, satellite communications, and 5G telecommunications. The primary function of these chips is to accurately set the relative gain and phase of each channel so that signals add coherently in the desired direction of the antenna main beam. They're being developed for analog phased-array applications or hybrid array architectures that combine some digital beamforming with analog beamforming.

The [ADAR1000](#) X-/Ku-band beamforming IC is a four-channel device covering 8 to 16 GHz, operating in time-division-duplex (TDD) mode with the transmitter and receiver integrated into one IC. In receive mode, input signals pass through four receive channels and are combined in a common RF_IO pin. In transmit mode, the RF_IO input signal is split and passes through the four transmit channels. *Figure 4* depicts a functional diagram.

A simple four-wire serial port interface (SPI) controls the on-chip registers. Two address pins allow SPI control of up to four devices on the same serial lines, while dedicated transmit and receive pins provide synchronization of all core chips in the same array. A single pin controls fast switching between the transmit and receive modes.

The four-channel IC is housed in a 7- × 7-mm QFN sur-



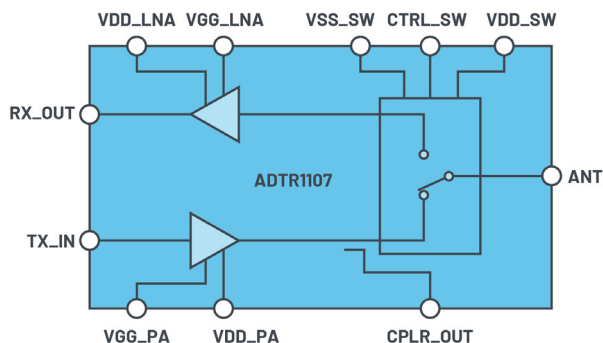
5. Here, we see plots of transmit gain/return loss (left) and phase/gain control (right) for the ADAR1000 beamforming IC, where frequency = 11.5 GHz.

face-mount package for easy integration into flat-panel arrays. The high level of integration coupled with a small package addresses some of the size, weight, and power challenges in high-channel-count phased-array architectures. The device dissipates only 240 mW/channel in transmit mode and 160 mW/channel in receive mode.

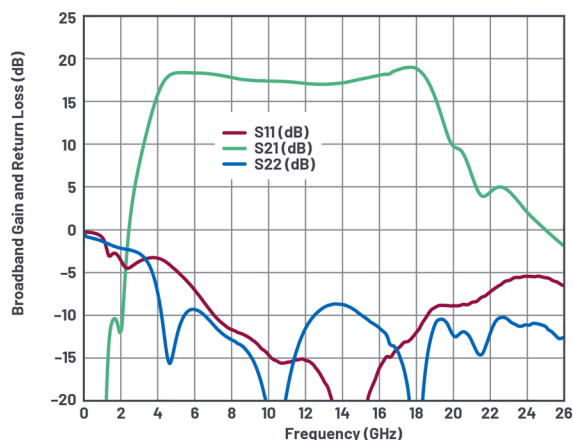
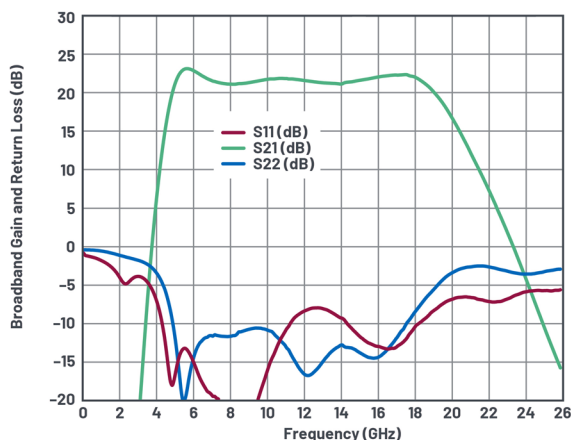
The transmit and receive channels are brought directly out of the beamforming IC package to the inputs of a front-end IC. Figure 5 shows plots of gain and phase for the device, which achieves full 360-degree phase coverage with phase steps less than 2.8 degrees and over 30 dB of gain adjustment. The ADAR1000 contains on-chip memory for storing up to 121 beam states, where one state contains all phase and gain

settings for the entire IC. The transmitter delivers approximately 19 dB of gain with 15 dBm of saturated power, while the receive gain is approximately 14 dB.

Another key metric is the phase change over gain setting, which is approximately 3 degrees over a 20-dB range. Simi-



6. This is a functional block diagram of the ADTR1107 front-end IC, which complements the ADAR1000 beamforming chip.



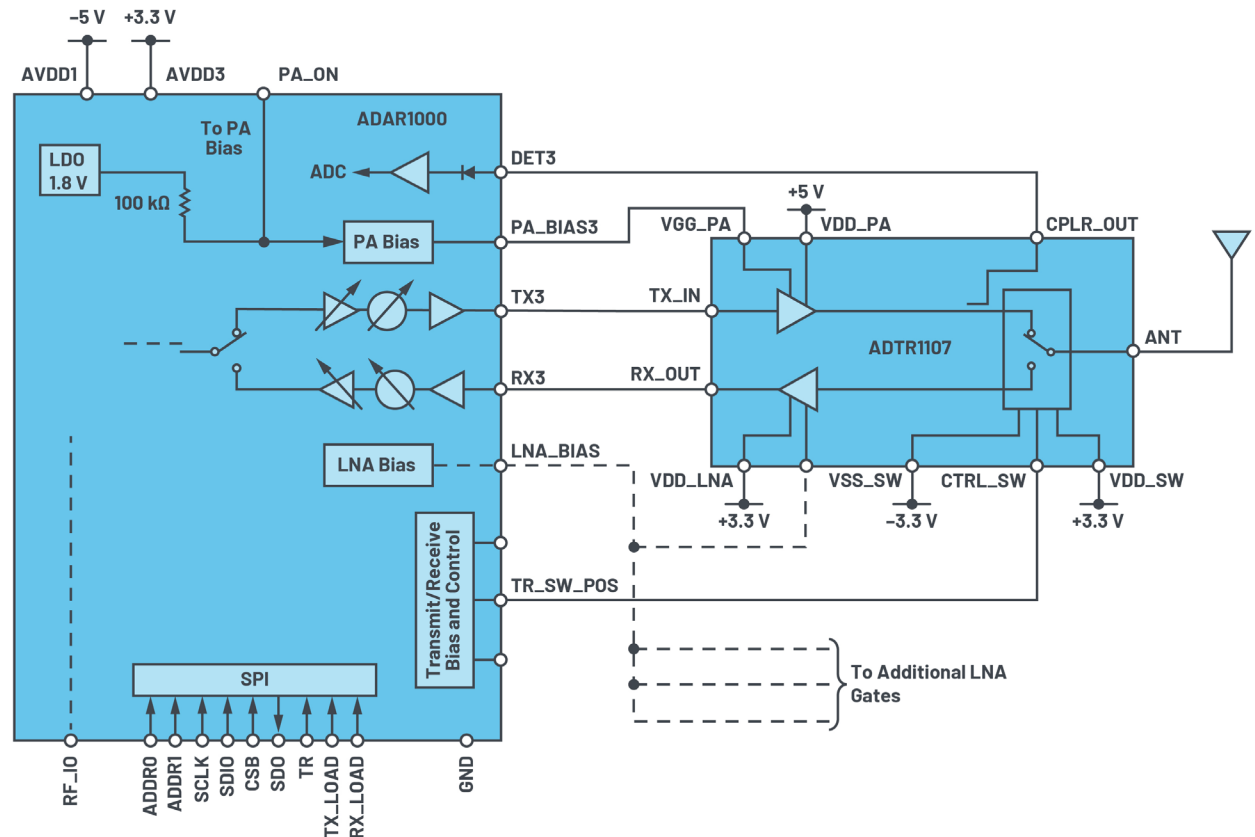
7. These plots depict the transmit gain/return loss (left) and receive gain/return loss (right) of the ADTR1107 front-end IC.

larly, the gain change with phase is about 0.25 dB over the entire 360-degree phase coverage, which eases the calibration challenges.

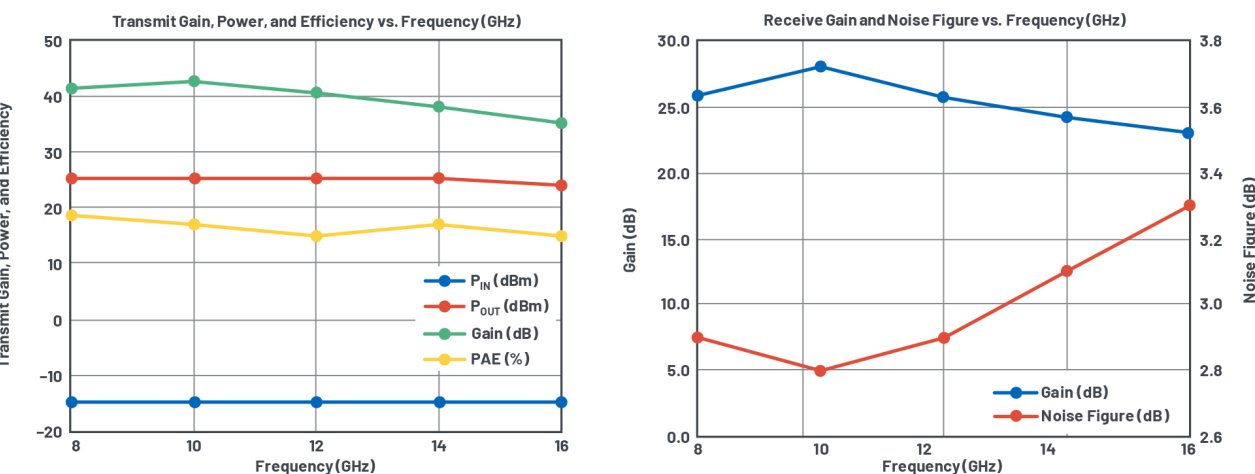
A complement to the ADAR1000 beamforming chip is the [ADTR1107](#) front-end IC. The ADTR1107 is a compact, 6- to 18-GHz, front-end IC with an integrated PA, LNA, and a reflective single-pole, double-throw (SPDT) switch. A function-

al block diagram is shown in *Figure 6*.

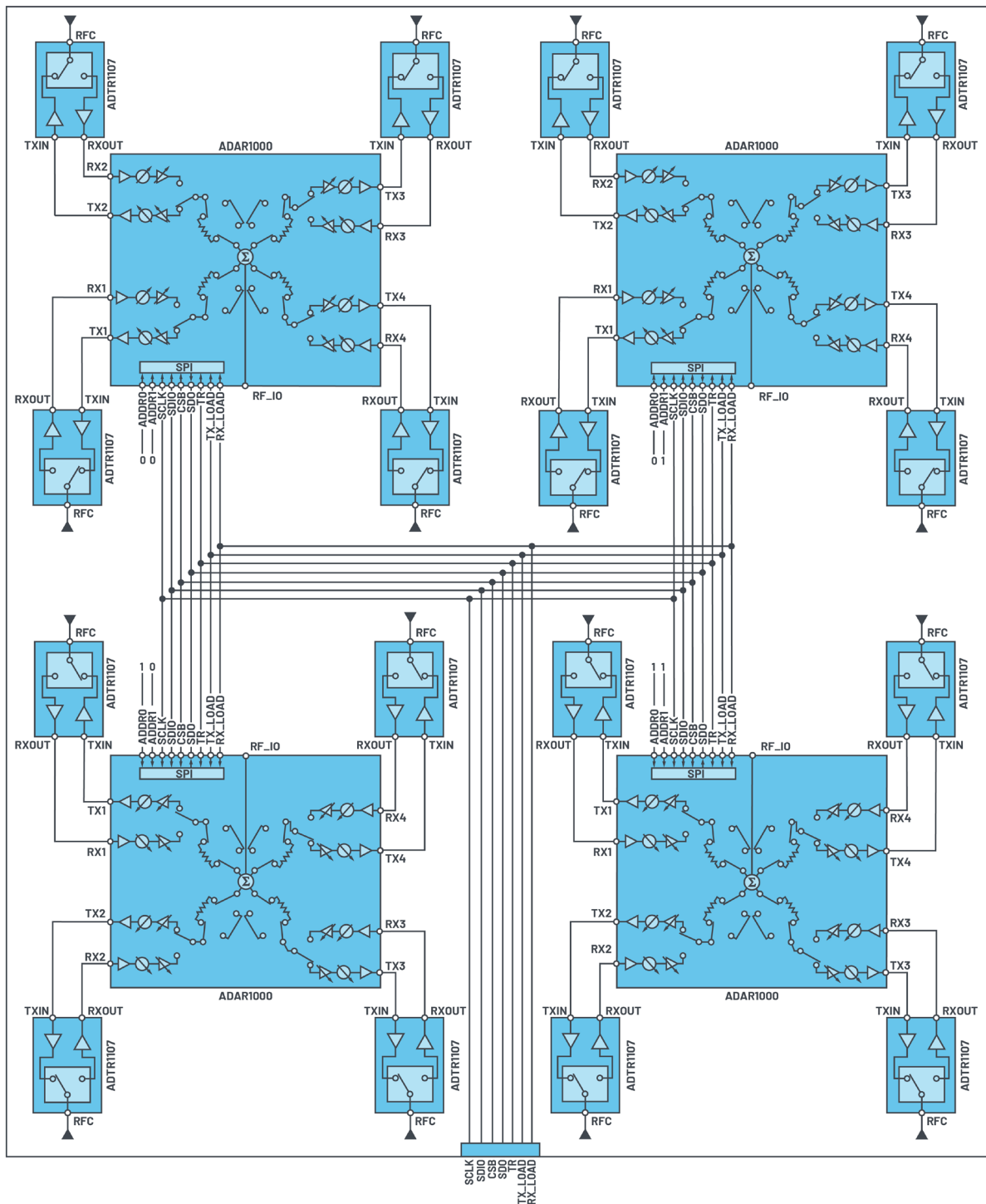
This front-end IC offers 25 dBm of saturated output power (PSAT) and 22 dB of small-signal gain in the transmit state. In the receive state, it provides 18 dB of small-signal gain and a 2.5-dB noise figure (including the T/R switch). The device has a directional coupler for power detection. The I/Os are internally matched to 50 Ω. The ADTR1107 comes in a 5- ×



8. Shown in this interface schematic are the links between the ADTR1107 front-end IC and the ADAR1000 X-band and Ku-band beamformer IC.



9. These plots illustrate the single channel transmit (left) and receive (right) performance of the ADTR1107 coupled with the ADAR1000.



10. Shown are four ADAR1000 chips driving 16 ADTR1107 chips; a simple four-wire SPI controls all of the on-chip registers.

5-mm, 24-lead, land-grid-array (LGA) package. The transmit and receive gain and return loss of the ADTR1107 are shown in Figure 7.

The ADTR1107 has been designed for easy integration with the ADAR1000; Figure 8 depicts an interface schematic. Four ADTR1107 ICs are driven by a single ADAR1000 core chip. For simplicity, we show the connections for only one of the four ADTR1107 ICs.

The ADAR1000 provides all of the required gate-bias voltages and control signals, resulting in a seamless interface to

the front-end IC. While the ADTR1107 LNA gate voltage is self-biased, the voltage can also be controlled from the ADAR1000. In addition, the gate voltage for the ADTR1107 power amplifier is provided by the ADAR1000.

Because one ADAR1000 drives four ADTR1107s, four independent negative gate voltages are needed for PA gate biasing. Each voltage is set by an 8-bit digital-to-analog converter (DAC). This voltage can be asserted by the ADAR1000 T/R input or by an SPI write. Asserting the ADAR1000 TR pin switches the polarity of the ADAR1000 between receive and

transmit modes. The TR_SW_POS pin can drive the gates of up to four switches and be used to control the ADTR1107 SPDT switch.

The ADTR1107 CPLR_OUT coupler output could be tied back to one of the four ADAR1000 RF detector inputs (DET1 to DET4 in *Figure 4*) to measure transmit output power. These diode-based RF detectors have an input range of -20 to $+10$ dBm. The coupling factor of the ADTR1107 directional coupler ranges from 28 dB at 6 GHz to 18 dB at 18 GHz.

One may achieve pulsing of the ADTR1107 via the gate voltage driven by the ADAR1000 while the drain is held constant. This is superior to pulsing via the drain, which would require a high-power MOSFET switch and gate-driver device, while gate switching requires only low currents. It should also be noted that the ADAR1000 puts out sufficient power to saturate the ADTR1107 in transmit mode, and the ADTR1107 is designed to survive the total reflected power in the case of a shorted antenna.

Figure 9 illustrates the combined performance of the ADTR1107 and the ADAR1000 in both transmit and receive modes over a frequency range from 8 to 16 GHz. In transmit mode, they provide approximately 40 dB of gain and 26 dBm of saturated power; in receive mode, they provide approximately 2.9 dB of noise figure and 25 dB of gain.

Figure 10 shows four ADAR1000 chips driving 16 ADTR1107 chips. A simple four-wire SPI controls all on-chip registers. Two address pins allow SPI control of up to four

ADAR1000 chips on the same serial lines. Dedicated transmit and receive load pins also provide synchronization of all core chips in the same array, and a single pin controls fast switching between the transmit and receive modes.

TRANSCEIVER CHIPSETS

Highly integrated RF transceiver chips contribute to more integration at the antenna level. One such example is the [ADRV9009](#), which offers a dual transmitter and receiver, integrated synthesizer, and DSP functions. The device includes a direct-conversion receiver with high dynamic range, wide bandwidth, error correction, and digital filtering built in.

Auxiliary functions include an analog-to-digital converter (ADC) and a DAC. General-purpose I/Os for the PA and RF front-end controls are also integrated. A high-performance phase-locked loop provides fractional-N RF frequency synthesis for the transmitter and receiver signal paths. The chip consumes very little power and includes power-down modes when not in use. The ADRV9009 comes in a 12×12 -mm, 196-ball chip scale ball-grid array.

Jeff Lane graduated from the University of Massachusetts with an M.S. degree in electrical engineering and has worked for Analog Devices since 2001. His experience includes microwave antenna design, systems engineering, sales, and marketing. He is currently a product marketing engineer in the Aerospace, Defense, and RF Products Group, focused mainly on RF and microwave MMIC amplifiers.

