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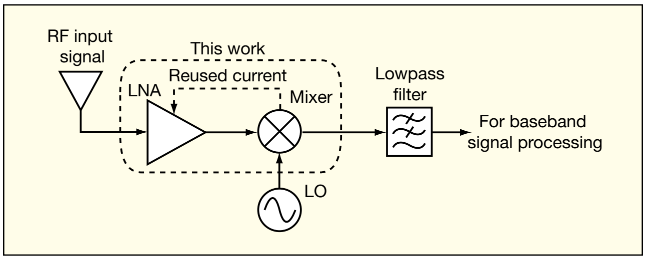
Low-Power Receiver

Serves Multiple Wireless Standards

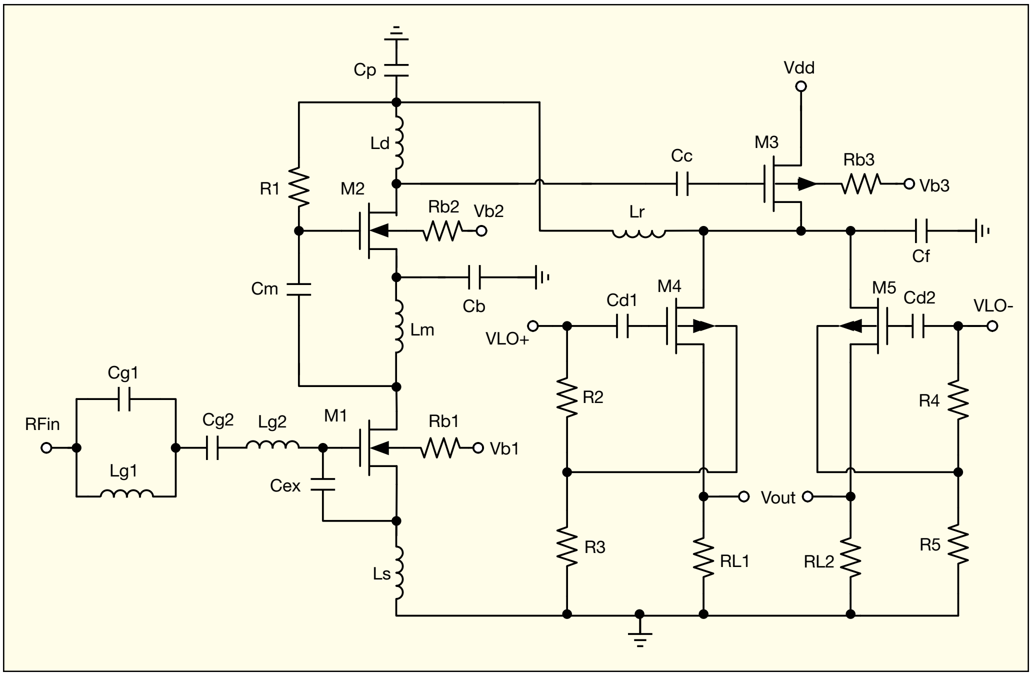
This extremely low-power front-end receiver design employs a current-reuse low-noise amplifier and switch-based single-balanced frequency mixer, achieving high conversion gain across its broad operating frequency range.

WIRELESS STANDARDS continue to emerge, with integrated-circuit (IC) radio designers challenged to handle as many of those standards as possible with a single solution. One such solution is a low-power integrated RF front end which uses a current-reuse low-noise amplifier (LNA) and a single-balanced mixer. The IC employs a double-resonant network for good input matching and reuses bleeding current from the mixer in the LNA for true low-power operation. The front-end IC is fabricated in a standard 0.18-μm silicon CMOS process and achieves conversion gain of 18.6 to 20.8 dB and double-sideband (DSB) noise figure of 2.3 to 5.1 dB across its operating bands. It draws only 2.1 mA current from a 1-V supply and measures 0.61 x 0.53 mm^2.

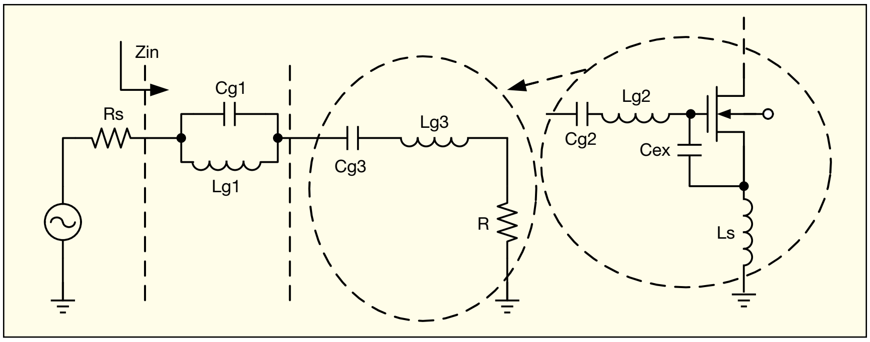
Given the rapid growth of wireless technology, the need for low-power radio electronics continues to increase rapidly—most notably, for remote and portable wireless applications using multiple radio standards. Silicon CMOS has been used in a number of low-power radio-frequency integrated circuits (RFICs) for wireless applications,[1-3] but often



1. This block diagram shows how the low-power receiver might be used in a communications system.



2. This is a more-detailed block diagram of the low-power receiver front end showing its circuit elements.



3. This is an equivalent-circuit diagram of the receiver's input circuitry and its double-resonator matching network.

in narrowband designs that are not suited for multiple-standard applications. In addition, many of these wireless CMOS RFICs are guilty of high power consumption, limiting their value for multiple-standard wireless applications.[4-9]

Minimizing power consumption usually involved reducing the supply voltage and current of a circuit. In the past, a conventional cascade structure (CS)[10] has been used in LNAs to optimize different performance parameters, including gain and reverse isolation. Nevertheless, this structure is not suitable for low-voltage applications since the supply voltage should be twice as large as the threshold voltage (V_{th}) of the LNA's transistors. A folded cascade CS topology proposed in ref. 11 operated at a supply voltage of only 0.7 V, but it induced more branch current and went against the ultra-low-power front-end design. A conventional cascade CS topology capable of reducing the supply voltage down to 0.6 V was unveiled in ref. 12, with good gain performance. However, the transistors in that configuration were working in a weak inversion region, which induced degradation of gain and noise-figure (NF) performance.[13]

Current-reuse topologies and forward-body-bias techniques have been used more recently to achieve low power consumption in RFICs.[1,13,14] But these efforts

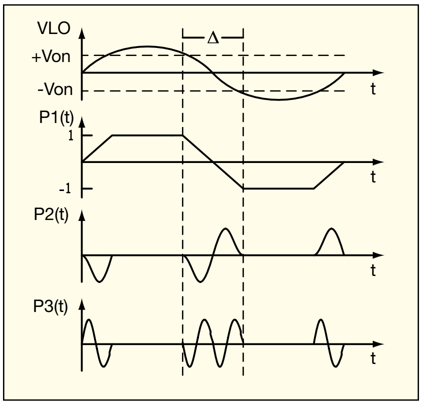
Table 1: Comparing communications bands.

Wireless standard	Frequency spectrum (MHz)	Centralized frequency spectrum (MHz)
GSM-900	935 ~ 960	935 ~ 960
DCS-1800	1805 ~ 1850	1805 ~ 2483
DECT	1881 ~ 1897	
PCS-1900	1930 ~ 1960	
TDS-CDMA	2010 ~ 2025	
WCDMA	2100 ~ 2170	
802.11b/g	2400 ~ 2483	
Bluetooth	2400 ~ 2483	

always focused on low-power LNA circuits—without inclusion of a low-power mixer—and often to the detriment of amplifier performance, such as linearity or NF. This current report applies current reuse and forward-body-bias techniques to the combination of an LNA and a mixer, improving the performance of both.

As **Table 1** shows, the frequency range of personal wireless communications standards is extensive. As a result, a double-resonant input matching network for the LNA/mixer was designed to resonate at center frequencies within 935 to 960 MHz and 1805 to 2483 MHz, respectively. The input architecture helps to achieve good impedance matching within these bands and to suppress noise between these two spans without an additional notch filter. The front-end circuit incorporates both current-reuse and forward-body-bias techniques to minimize current consumption at low supply voltages. The circuit reuses bleed current from the mixer to energize the LNA[15] and a local-oscillator (LO) signal forward-body-bias technique to minimize current draw.

Figure 1 shows the block diagram of an ultra-low-power RF receiver. RF input signals enter the LNA from the antenna. The LNA amplifies these voltage input signals by reusing bleed current from the mixer. Amplified signals from the LNA enter the single-balanced mixer and are mixed with the LO signals. The intermediate-frequency (IF) output signals from the mixer are processed by the lowpass filter. Finally, the



4. These plots show the resulting waveforms for P1(t), P2(t), and P3(t) for an applied LO voltage.

filtered signals enter the baseband signal system for further processing.

Figure 2 shows the proposed multiple-standard low-power CMOS RF receiver front-end circuit. It contains a stacked NMOS LNA and a single-balanced PMOS mixer. To minimize power consumption, the front-end employs current-reuse and forward-body-bias techniques, although these techniques will not degrade noise figure or linearity. Traditional multiple-standard receivers usually gained good input impedance matching by means of a wideband matching network[5] or tunable frequency matching network.[16] The former will induce some extra interference in some useless frequencies, which are covered by the wideband matching network; the latter increases the operating complexity of the circuits. The front-end circuit adopts a double resonance matching network to realize the multiple-standard input impedance matching.

As shown in **Fig. 2**, the parallel $L_{gl} - C_{gl}$ and series $L_{g2} - C_{g2}$ resonances are series connected. For design flexibility, a source degeneration inductor, L_S, is placed in series with the source. a capacitor, C_{ex}, is added in parallel with the gate-source of the amplifying transitor, M1.

In **Fig. 3**, the source degenerate topology is replaced by its equivalent circuit. The input impedance can be expressed as:

(See Eq. 1, this page.)

where:

g_{ml} = the transconductance of M1 and
C_{gs1} = the gate-source capacitance of M1.

The values of capacitor C_{g3} and inductor L_{g3} can be calculated by Eqs. 2 and 3:

$$C_{g3} = \frac{C_{g2} \cdot (C_{gs1} + C_{ex})}{C_{g2} + (C_{gs1} + C_{ex})} \quad (2)$$

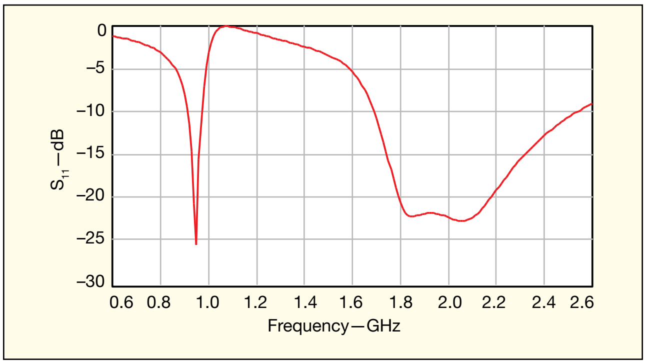
$$L_{g3} = L_{g2} + L_s \quad (3)$$

Parameter Z_{in} synthesizes an input impedance with a real part equal to $g_{m1}L_S/C_n$ where capacitance $C_n = C_{ex} + C_{gs}$, to be matched with source resistance, $R_S = 50\ \Omega$.

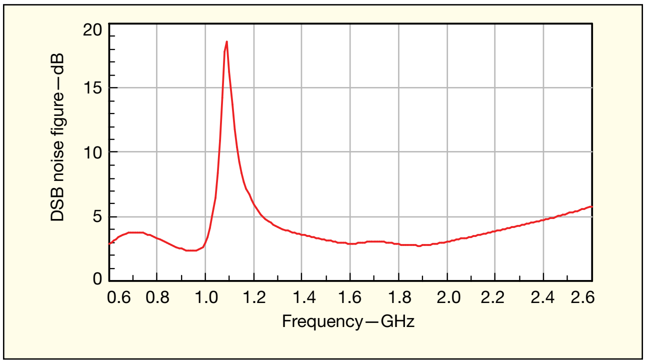
To achieve the required input impedance matching at the desired frequency bands, resonances $L_{gl} - C_{gl}$ and $L_{g3} - C_{g3}$ are designed to resonate at center frequencies within 935 to 960 MHz and 1805 to 2483 MHz,

$$Z_{in} = S\left(\frac{L_{g1}}{C_{g1} \cdot L_{g1} + 1}\right) + \frac{1}{SC_{g3}} + SL_{g3} + \frac{g_{m1}L_s}{(C_{gs1} + C_{ex})} \quad (1)$$

$$A_1 = \frac{v_{d1}}{v_{in}} = \frac{g_{m1}}{\omega_0 \cdot SC_{gs1}} \cdot \frac{1}{R_{in}}\left(SL_m // R_1 // \frac{1}{SC_{out1}}\right) \quad (4)$$



5. The front-end receiver's S_{11} input-reflection-coefficient response was simulated from 0.6 to 2.6 GHz.



6. The front-end receiver's double-sideband (DSB) noise figure was simulated from 0.6 to 2.6 GHz.

respectively. In this way, the input circuit not only accomplishes better impedance matching in both bands of 935 to 960 MHz and 1805 to 2483 MHz, but also suppresses interference within the middle band from 960 to 1805 MHz without using an additional notch filter. The values of the resonating inductors and capacitors can easily be calculated by using the equation $\omega = 1/2\pi(LC)^{0.5}$.

To achieve a low-power design, the current-reuse technique was used twice in the front-end circuit. In one instance, it was applied to the two-stage cascade common-source LNA. As was shown in **Fig. 2**, the signal amplified by device M1 is coupled to the gate of device M2 by capacitor C_m while the source of M2 is bypassed by capacitor C_b. The inductive load L_m and L_D of the first and second amplifier stages can help to achieve high power gain; the supply voltage will not be influenced, as the voltage drop across them is negligible. Resistor R1 is added to supply a DC bias for device M2. By applying M1 and M2 to share the same bias current, the power consumption of the LNA is minimized. Body effects and parasitic capacitances are not considered. The voltage-transfer function of the first and second stages can be expressed by Eqs. 4 and 5:

(See Eq. 4, p. 54.)

$$A_2 = \frac{v_{d2}}{v_{d1}} = g_{m2}(r_{o2} // SL_d // \frac{1}{SC_{out2}}) \quad (5)$$

where:
C_{outn} = the output capacitors (where n = 1, 2) for M1 and M1;
r_{on} = the output resistance for M1 and M2; and
ω_0 = the working frequency.

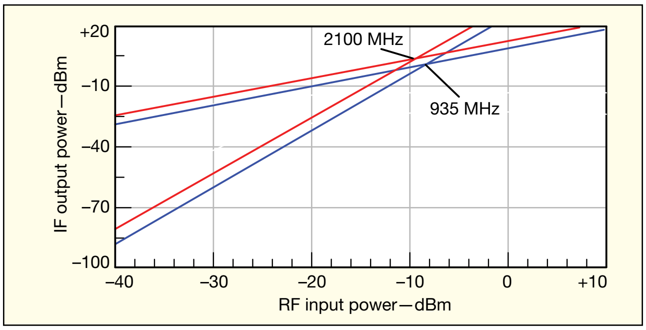
The supply current of the LNA is obtained from the bleed current of the mixer, rather than from the DC source. By doubling the instance of current reuse, current consumption is minimized while bleeding current from the mixer helps to improve the conversion gain of the mixer. Device M3 is the transconductance transistor, while C_p and C_c are bypass and coupling capacitors, respectively. Inductor L_r and parasitic capacitance C_f at the common source node of the mixer's switching transistors, M4 and M5, are chosen for values to improve interstage impedance matching between the LNA and mixer. The $L_r - C_f$ resonance also helps to suppress 1/f noise at the mixer's output. Resistors R_{L1} and R_{L2} are load resistors. The conversion voltage gain of the mixer can be found from Eq. 6:

$$A_3 = (2/\pi)g_{m3}R_L \quad (6)$$

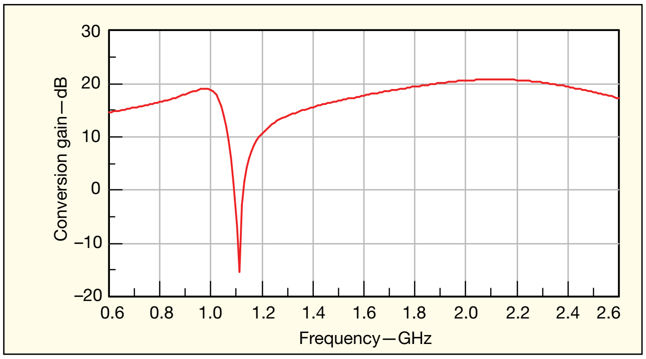
Therefore, the overall voltage conversion gain of the RF front end can be calculated from Eq. 7:

$$A = A_1 \cdot A_2 \cdot A_3 \quad (7)$$

To achieve further savings in power consumption and ensure the feasibility



7. The conversion gain of the front-end receiver was simulated from 0.6 to 2.6 GHz.



8. The input third-order-intercept (IIP3) response of the front-end receiver was simulated at 935 and 2100 MHz.

of current reuse between the LNA and the mixer, the supply voltage of the LNA and mixer should be decreased. Usually, the conventional method for accomplishing this is by making the transistors work in their weak inversion regions, although this can degenerate noise figure and gain performance levels. Thus, the forward-body-bias technique is applied to solve this weak point. Typically, the threshold voltage (V_{th}) equations for both NMOS and PMOS transistors are given as[13]:

$$V_{thn} = V_{th0} + \gamma(\sqrt{2\varphi_f - V_{bs}} - \sqrt{2\varphi_f}) \quad (8)$$

$$V_{thp} = V_{th0} - \gamma(\sqrt{2\varphi_f + V_{bs}} - \sqrt{2\varphi_f}) \quad (9)$$

where:
V_{th0} = the threshold voltage when $V_{bs} = 0$;
γ = the body-effect coefficient;
ϕ_f = the bulk Fermi potential; and
V_{bs} = voltage between the body and source.

From Eqs. 8 and 9, V_{th} can be modified by changing V_{bs}. Thus, the MOS transistors can achieve a dynamic threshold voltage. Since a forward body bias effectively lowers the threshold voltage, the MOS transistors can operate at a reduced bias voltage while maintaining equivalent device characteristics in terms of gain, noise figure, and linearity. However, as the forward body bias turns on the source-to-body junction of the MOS transistors, a DC current flows across the junction with an exponential dependence on the body voltage, leading to additional power consumption and possible latch-up failure. To prevent excessive junction conduction, a current-limiting resistor should be included at the body terminal.

By adding suitable positive voltages (V_{b1} and V_{b2}) and current-limiting resistors (R_{b1}, R_{b2}) to the body terminals of devices M1 and M2, a forward-body-bias architecture is formed in the front end. From Eq. 8, with the increase of V_{bs} and the decrease of V_{thn}, the NMOS transistors can work in a strong inversion region under low-bias-voltage conditions. The stacked NMOS LNA can operate at reduced supply voltages as low as 0.6 V, which is convenient to reuse the bleeding current when the supply voltage is equal to the drain voltage of transconductance transistor M3.

A positive voltage (V_{b3}) and a current-limiting resistor (R_{b3}) are added to the body terminal of PMOS transistor M3. As Eq. 9 shows, V_{bs} is then increased and V_{thp} is decreased, so that the PMOS transistors also work in a strong inversion region under low-supply-voltage conditions.

The mixer employs a novel forward-body-bias method for the switching transistors. The mixer is heavily dependent on the ideal characteristics of the switching transistors, so a local-oscillator (LO) signal forward-body-bias technique is adopted to improve the switching characteristics of devices M4 and M5. The LO voltage is connected to the body terminals of transistors M4 and M5, which can maintain the same waveform and phase, and reduce the voltage amplitude by divider resistors R2/R3 and R4/R5. The body voltage is then cyclical changed with the LO signal, which can be determined by means of Eq. 10:

$$V_{LO+} = V_{LO-} = V_{bs}\cos(\omega_{LO}t) \quad (10)$$

From Eq. 9, when $V_{LO+} > 0$ and $V_{LO-} < 0$, the value of V_G for device M4 increases, and $|V_{GS}|$ declines and $|V_{thp}|$ increases, accelerating the PMOS transistor to satisfy

Table 2: Reviewing recently reported multiple-standard receivers.

Reference	5	6	7	8	9	This work
Contents	LNA	LNA + mixer	LNA + mixer	LNA	LNA	LNA + mixer
Bandwidth (GHz)	0.2 ~ 3.8	2 ~ 6	0.8 ~ 2.5	3 ~ 6.5	3 ~ 10	0.93 ~ 0.96/ 1.8 ~ 2.5
Noise figure (dB)	2.8 ~ 3.4	3.18 ~ 5.47	< 6	1.9 ~ 3.4	3 ~ 7	2.3 ~ 2.4/ 2.7 ~ 5.1
S_{11} (dB)	< –9	< –10		< –12	< –9	< –14/< –11
Gain (dB)	19	35	20 ~ 21.5	16	12.5	18.6 ~ 19.0/ 18.7 ~ 20.8
IIP3 (dBm)	–4.2	–17.4 ~ –11.3	–20			–8.2/–9.8
Supply (V)	1	1.8	1.8	1.06	1.2	1
Power (mW)	5.7	56	18	4.5	7.2	2.1
Technology	0.13 µm	0.18 µm	0.18 µm	0.18 µm	90 nm	0.18 µm

the cutoff condition that $|V_{GS}| < |V_{thp}|$. Device M4 enters the cutoff state quickly.

At the same time, the value of V_G for device M5 declines, $|V_{GS}|$ increases and $|V_{thp}|$ declines, accelerating the PMOS transistor to satisfy the turn-on condition, $|V_{GS}| > |V_{thp}|$ and device M5 enters the turn-on state quickly. The LO signal is coupled to the body terminal and enables the threshold voltage to change in a cyclical manner. This not only helps the mixer to work at low power consumption, but also raises the switching speeds of the transistors. The switching characteristics of the active devices is nearly ideal, and the noise figure and linearity are improved considerably.

The thermal noise is greatly generated when switching transistors turn-on simultaneously. The average noise current within one LO period can be expressed by means of Eq. 11:

$$i_{o,n} = 4I[V_n/(S \times T)] \quad (11)$$

where:

V_n = the 1/f noise of the MOS transistor;
T = the cycle time of the LO;
I = the DC current of the switching transistor; and
S = the LO signal slope at point zero.

Parameter S is critical to noise performance: a larger value of S means smaller noise current. Parameter S can be increased to improve the switching characteristic, so it is propitious to reduce noise current. Linearity is an important performance of RF front-end, especially for the last stage of the whole circuit. Thus, the linearity of this front-end circuit is greatly influenced by the switching transistors M4 and M5. Their output current, i_0, has a nonlinear relationship with input voltage v_s, which can use the Taylor series to expand as shown in Eq. 12:

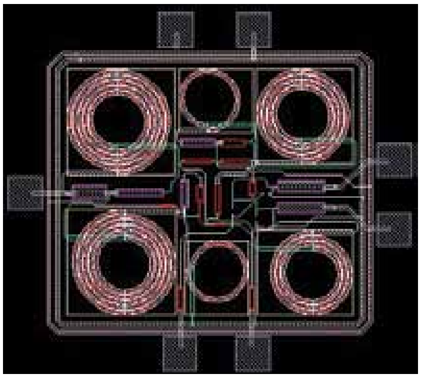
$$i_o = p_1(t) \cdot v_s + p_2(t) \cdot v_s^2 + p_3(t) \cdot v_s^3 + \cdots \quad (12)$$

From Eq. 12, where p_n is the derivative of i_0 ~ V_s, the typical waveform is shown in **Fig. 4**. When the switching transistor is on, $p_1(t) = 1$, $p_2(t) = p_3(t) = 0$, while in the switching time period Δ, $p_1(t)$, $p_2(t)$, $p_3(t)$ are unequal to zero. The voltage mode for the input third-order intercept point, V_{IIP3}, can be analyzed by means of Eq. 13:

$$V_{IIP3} = 10\log[4|p_1|/3|p_3|] \quad (13)$$

From Eq. 13, it can be concluded that smaller values of $|p_3|$ mean higher IIP3 and better linearity. With the aid of the LO signal forward-body-bias technique, the switching time, Δt, is reduced, implying that the time for $|p_3| \neq 0$ is reduced and the IIP3 performance has been enhanced.

The RF receiver front-end design was implemented in the 0.18-µm silicon CMOS process at the foundry of the Taiwan Semiconductor Manufacturing Company (TSMC; www.tsmc.com). By using the forward-body-bias technique, the receiver's supply voltage drops to 1 V when the forward body bias voltages are chosen



9. This chip photograph shows the basic layout of the dual-band receiver, fabricated in a commercial silicon CMOS foundry.

at $V_{b1} = V_{b3} = 0.4$ V and $V_{b2} = 0.35$ V. Operating across the frequency ranges of 935 to 960 MHz and 1805 to 2483 MHz, the input reflection coefficients S_{11} for those frequency ranges are less than –14 and –11 dB, respectively, as shown in **Fig. 5**.

The double-sideband (DSB) noise figures range from 2.3 to 2.4 dB and 2.7 to 5.1 dB, respectively, across those two frequency bands, as shown in **Fig. 6**. The conversion gains for the two frequency ranges are 18.6 to 19.0 dB and 18.7 to 20.8, respectively **(Fig. 7)**. The input third-order-intercept points (IIP3) for the front end are –8.2 dBm at 935 MHz and –9.8 dBm at 2100 MHz **(Fig. 8)**. **Figure 9** shows the layout for the front end, with an active area of 0.61 x 0.53 mm^2. The power consumption is only 2.1 mW. **Table 2** summarizes the performance of the front-end device.

The total measured conversion gain of the receiver is 18.6 to 20.8 dB and the DSB noise figure ranges from 2.3 to 5.1 dB. The IIP3 is –8.2 dBm at 935 MHz and –9.8 dBm at 2100 MHz. Power consumption is a mere 2.1 mW with a 1-V supply. MWRF

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REFERENCES

1. J. Liu, H. Liao, and R. Huang, "0.5 V ultra-low power wideband LNA with forward body bias technique," Electronics Letters, Vol. 45, No. 6, 2009, pp. 289-290.
2. T.T.N. Tran, et al., "Ultra-low-power series input resonance differential common gate LNA," Electronics Letters, Vol. 47, No. 12, 2011, pp. 703-704.
3. W. Dake, et al., "A 0.4-V Low Noise Amplifier Using Forward Body Bias Technology for 5 GHz Application," IEEE Microwave and Wireless Components Letters, Vol. 17, No. 7, 2007, pp. 543-545.
4. A. Chyuen-Wei, Z. Yuanjin, and H. Chun-Huat, "A Multi-band CMOS Low Noise Amplifier for Multi-standard Wireless Receivers," in ISCAS 2007 IEEE International Symposium on Circuits and Systems.
5. W. Hongrui, Z. Li, and Y. Zhiping, "A Wideband Inductorless LNA With Local Feedback and Noise Cancelling for Low-Power Low-Voltage Applications," IEEE Transactions on Circuits and Systems I: Regular Papers, Vol. 57, No. 8, 2010, pp. 1993-2005.
6. W. Chao-Shiun, L. Wei-Chang, and W. Chorng-Kuang, "A multi-band multi-standard RF front-end IEEE 802.16a for IEEE 802.16a and IEEE 802.11 a/b/g applications," in IEEE 2005 International Symposium on ISCAS.
7. N. Mingchen, et al. "A wide-band RF front-end for multi-standard application," in 9th International Conference on Solid-State and Integrated-Circuit Technology, ICSICT 2008.
8. L. Chen-Ming, et al., "A Low-Power Self-Forward-Body-Bias CMOS LNA for 3-6.5-GHz UWB Receivers," IEEE Microwave and Wireless Components Letters, Vol. 20, No. 2, 2009.

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