Design Feature

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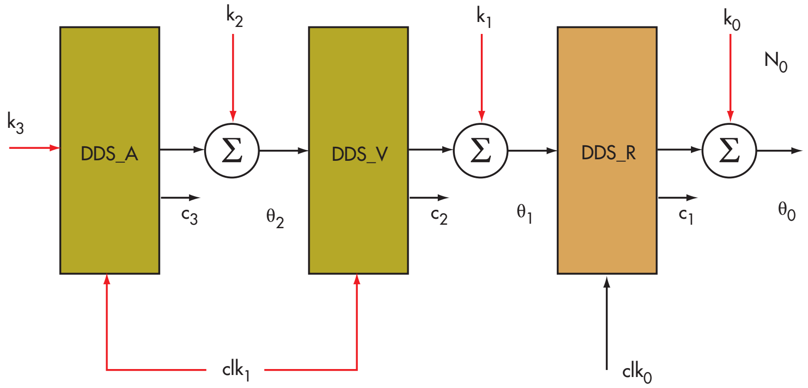
DDS Model Tunes Doppler Simulation

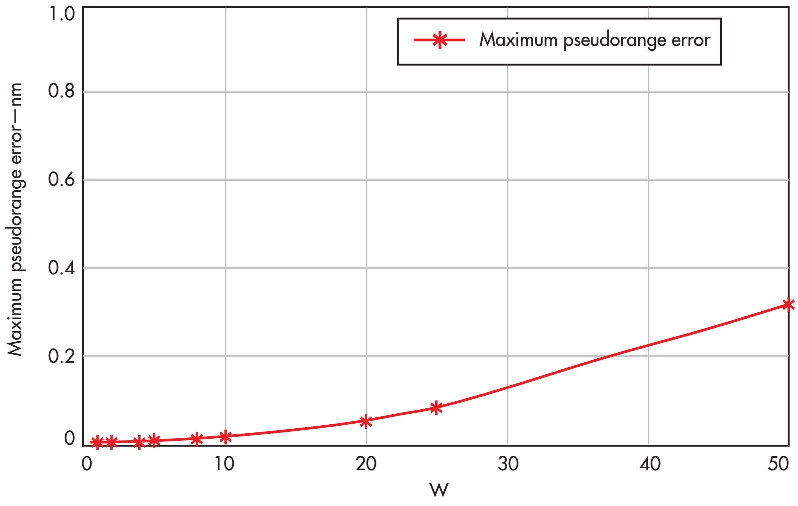
An accurate model for a third-order direct-digital synthesizer can be used for computer simulations of satellite navigation receivers under different conditions.

Testing satellite navigation receivers usually depends on signal simulation to evaluate a satellite navigation receiver under high-dynamic-range conditions.[1,2] A third-order direct-digital synthesizer (DDS) is invaluable for such simulation and testing, and the accumulation clock rate for each of the three DDS stages can either be the same or different. Numerous reports have been based on the use of same-clock conditions for these multiple-stage DDS sources,[3,4] with few studies of higher-order, hybrid-clock DDS sources, structured with multiple cascade accumulators with different accumulation clock rates.[5] To better understand these hybrid-clock, third-order DDS sources, a simulation model was developed and a model was derived for its output phase behavior. Hopefully, the straightforward model can be applied to better understand the application of DDS sources in phase-sensitive applications, including for use in satellite navigation receivers.

The performance and versatility of high-frequency DDS sources has been well documented in recent years for a wide range of applications in commercial, industrial, and military markeets. These are signal sources that are capable of reasonably low phase noise and overall excellent spectral purity, with oiutstanding switching speed over fairly wide frequency tuning ranges. The function of a DDS accumulator can be expressed as a simple relationship (Eq. 1), where the output of the DDS accumulator is represented as acc(n), with n as the clock number index, n_0 as the clock number when the accumulator resets, x as the initial value,



1. This diagram represents the hybrid-clock third-order DDS model.



2. This plot shows maximum pseudoranging errors for different values of W.

and k as the accumulation step.[4] When the DDS accumulator is implemented in a field-programmable gate array (FPGA), the output always lags behind the input by one clock cycle.

$$acc(n) = \begin{cases} x & n = n_0 \\ x + \sum_{m=n_0+1}^{n} k(m) & n > n_0 \end{cases} \quad (1)$$

Figure 1 shows a third-order, hybrid-clock DDS model with three cascaded DDS accumulators (defined as DDS_A, DDS_V, and DDS_R, respectively). The first stage accumulator runs with a different accumulation clock rate from the other two accumulators.

Parameters k_0 through k_3 are the initial accumulation parameters of each accumulator stage; parameters θ_0 through θ_2 are the outputs of each different accumulator stage; N_0 is the word length of parameter k_0; and c_1 through c_3 are the bits that must be truncated when adding the accumulator output to the initial accumulator parameter. Parameters clk_0 and clk_1 are clock signals driving the first and additional accumulator stages, respectively, as represented in Eq. 2:

$$clk_0 = W \times clk_1 \quad (2)$$

In Eq. 2, the clock frequency division coefficient, $W \geq 1$, is an integer. In the case of $W = 1$, the DDS model degenerates into the same-clock model presented in ref. 4.

Based on the model of *Fig. 1*, the output of each accumulator stage can be derived when W is an unknown parameter. The output of the last stage DDS, DDS_R—supposing the number of the accumulation clock is n, $Y = [n/W]$, where the square brackets denote rounding the contained value to an integer—results in Eq. 3:

See Eq. 3 on p. 74.

For a satellite navigation signal simulator, a simulated signal Doppler is

ANALYZING A SINGLE THIRD-ORDER DDS

Clock frequency division coefficient W	Occupied slice	Static power consumption(mW)	Dynamic power consumption (mW)
1	221	97	39
10	204	95	4

generated due to radial variable motion between the receiver and satellite. The relationship of parameters in the model must satisfy the conditions presented in Eq. 4.[4]:

$$p(n) = \frac{f_T}{c}\left(R + \frac{v}{f_c}n + \frac{a}{2f_c^2}n^2 + \frac{\hat{a}}{6f_c^3}n^3\right) \quad (4)$$

where:

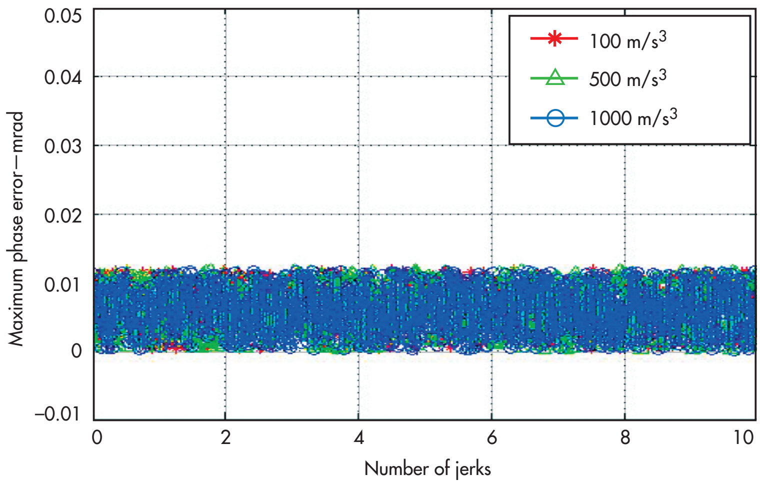
R = the initial pseudorange amount;
v = the initial velocity;
a = the accelerated velocity;
â = the amount of jerk;
f_T = the transmit signal frequency; and
f_c = the clock rate of DDS_R.

In order to obtain initial accumulation parameters k_0 through k_3), it can be presumed that the output phase of the third-order DDS satisfies Eq. 5 at n = 0, W, 2W…iW for i ∈ Z+:

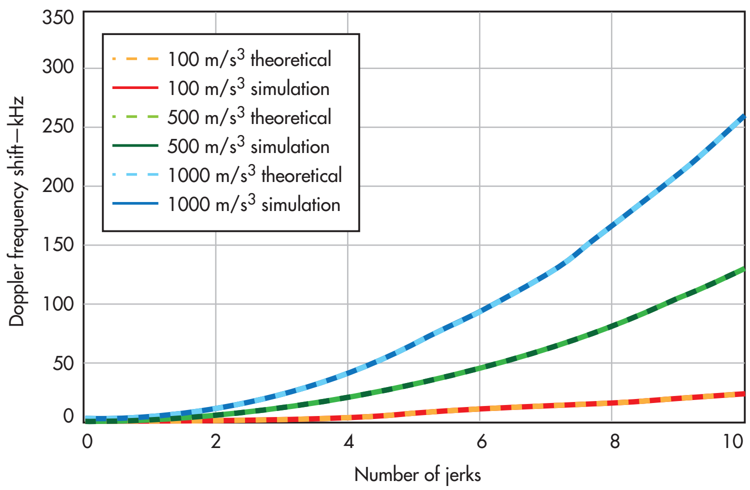
$$p(iW) = \frac{\theta_0(iW)}{2^{N_0}} \quad (5)$$

If Eq. 5 is the constraint condition, and N_0 and c_0 through c_3 are treated as known parameters, the values of k_0 through k_3 in Eq. 3 can be obtained by means of Eq. 6:

See Eq. 6 on p. 74.



3. These are simulation results for maximum phase errors with different amounts of jerk applied.



4. These are simulation results of Doppler frequency shifts with different jerk rates applied.

To prove that Eq. 6 satisfies Eq. 5 at any i ∈ Z+, mathematical induction can be applied. The proven steps are easily derived.

Compared with the results of ref. 4, the calculation results of the same-clock condition is the case of W = 1 in Eq. 6, and when W > 1, the hybrid-clock third-order DDS will generate a larger pseudorange error than a same-clock DDS. In case of f_c = 100 MHz and W ≤ 50, and ignoring word-length quantization errors, the third-order DDS output pseudorange errors under the high-dynamic-range conditions represented by v = 1000 m/s; a = 1000 m/s^2; and â = 1000 m/s^3 will be simulated.

For a third-order DDS simulation run time of 10 ms, *Fig. 2* shows the maximum pseudorange errors that will occur for different values of the accumulator variable W. According to this simulation, as the value of parameter W increases, the maximum pseudorange error caused by the hybrid clock increases correspondingly. In the case of values of W ≤ 10, the maximum pseudorange error is smaller than 10^{-10} m.

As part of an analysis, Doppler simulation errors for the hybrid-clock third-order DDS can be mainly attributed to the quantization error of the word length at each stage. Therefore, the word length of each accumulator stage must be designed accordingly, to minimize quantization errors. In Eq. 7, parameters ΔR, Δv, Δa, and Δâ represent the resolution of the pseudorange, the velocity, the acceleration, and the jerk amount, respectively. For the case of k_i = 1, the corresponding parameter should be smaller than the resolution. The word length obtained from Eq. 6 can be expressed in terms of Eq. 7:

$$\begin{cases} N_0 = \left[lb \dfrac{c}{f_T \Delta R} \right], \\ c_1 = \left[lb \dfrac{cf_c}{f_T \Delta v} \right] - N_0, \\ c_2 = \left[lb \dfrac{cf_c^2}{f_T \Delta a W} \right] - N_0 - c_1, \\ c_3 = \left[lb \dfrac{cf_c^3}{f_T \Delta \hat{a} W^2} \right] - N_0 - c_1 - c_2, \end{cases} \qquad (7)$$

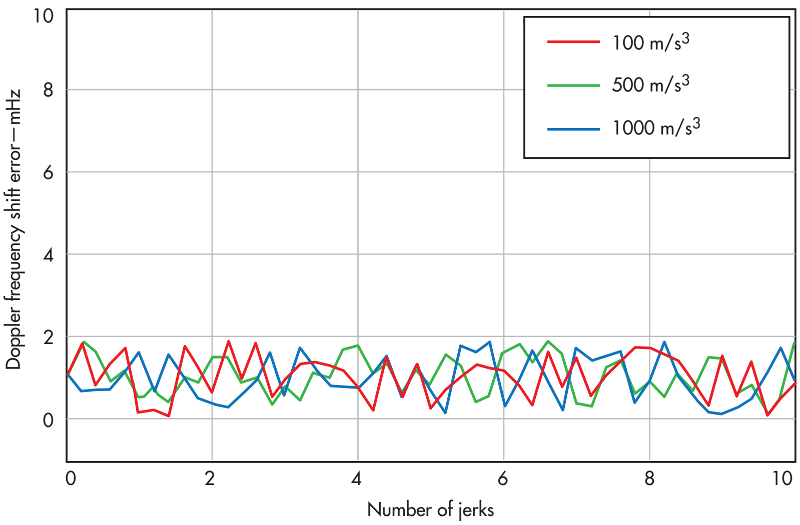
The square brackets in Eq. 7 represent rounding to an integer value. It should be evident from Eq. 7 that the lower bounds of word length parameters for all three accumulators are $N_0 + c_1$, $N_0 + c_1 + C_2$, and $N_0 + c_1 + c_2 + c_3$, respectively.

When W = 1, Eq. 7 reverts to the results for a same-clock third-order DDS. Considering the initial accumulation parameter calculation expressions, it is clear that the same-clock third-order DDS simulation model can be unified with the hybrid-clock simulation model, and the word length obtained when W > 1 is shorter than the one when W = 1.

Using a 1561.098-MHz BeiDou2 B1 carrier signal simulation as an example,[6] the reductions in word length can be analyzed while W > 1. For this example, the sampling frequency is assumed to be 100 MHz, the clock frequency division coefficient W can be 1 or 10, $\Delta R = 5$ cm, $\Delta v = 1$ mm/s, $\Delta a = 10$ mm/s^2, and $\Delta\hat{a} = 10$ mm/s^3. The values of $N_0 = 2$ and $c_1 = 33$ do not matter whether W = 1 or 10. For $c_2 = 23$ and $c_3 = 26$ when W = 1 and $c_2 = 20$ and $c_3 = 23$ when W = 10, three bits of resolution are reduced at each DDS stage.

The model was used to simulate the performance of a hybrid-clock third-order DDS. Simulation parameters were similar to those used previously, with W = 10, and with word-length parameters of $N_0 = 6$, $c_1 = 33$, $c_2 = 20$, and $c_3 = 23$. With an initial velocity of 0, the acceleration is 0 m/s^2, and the jerk rates are 100 m/s^3, 500 m/s^3, and 1000 m/s^3, respectively. To avoid errors from a long accumulation period, caused by DDS word-length quantization, the hybrid-clock, third-order DDS is initialized every other 10 ms during simulation. Under different jerk amounts, the maximum phase error at every 10-ms simulation interval is always less than 0.02 mrad (*Fig. 3*).

During this simulation, the phase sequence of the DDS_R within each simulation interval is obtained; a direct phase modeling method was adopted to estimate the Doppler frequency shift produced.[7] The simulation results are shown in *Fig. 4* and the corresponding Doppler frequency-shift errors in *Fig. 5*. The simulation results are compared to the theoretical values (the dashed lines) and how they line up for different jerk rates, and with data sampling intervals in both figures increased to 200 ms. The jerk rates in both cases are presented as the number of jerks per second, from 0 to 10, with the higher jerk rates resulting in more significant Doppler frequency shifts. This span of jerk rates allows designers to gauge expected performance for an FPGA in a DDS application when subjected to different conditions.



5. This plot shows simulation errors of Doppler frequency shifts with different jerk rates applied.

$$
\begin{aligned}
\theta_0(n) &= k_0 + \sum_{j=1}^{n} \theta_1(j-1)/2^{c_1} \\
&= k_0 + [W \sum_{i=1}^{Y} \theta_1(j-1) + (n-YW)\theta_1(Y)]/2^{c_1} \\
&= k_0 + \frac{YWk_1}{2^{c_1}} + \frac{k_2W(Y^2-Y)}{2\times 2^{c_1+c_2}} + \frac{Wk_3(Y^3-3Y^2+2Y)}{6\times 2^{c_1+c_2+c_3}} \\
&\quad + \frac{(n-YW)k_1}{2^{c_1}} + \frac{(n-YW)Yk_2}{2^{c_1+c_2}} + \frac{(n-YW)k_3(Y^2-Y)}{2\times 2^{c_1+c_2+c_3}} \\
&= k_0 + \frac{nk_1}{2^{c_1}} + \frac{k_2(2Yn-WY-Y^2W)}{2\times 2^{c_1+c_2}} + \frac{k_3W(Y^3-3Y^2+2Y)+k_3 3(n-YW)(Y^2-Y)}{6\times 2^{c_1+c_2+c_3}} \\
&= k_0 + \frac{nk_1}{2^{c_1}} + \frac{k_2(2Yn-WY-Y^2W)}{2\times 2^{c_1+c_2}} + \frac{k_3(3nY^2-2Y^3W-3nY+2WY)}{6\times 2^{c_1+c_2+c_3}} \\
&\quad (n \geq 0)
\end{aligned}
\tag{3}
$$

$$
\begin{cases}
k_0 = \dfrac{f_T}{c} R \times 2^{N_0} \\
k_1 = \dfrac{f_T}{c}\left(\dfrac{v}{f_c} + \dfrac{a}{2f_c^2}W + \dfrac{\hat{a}}{6f_c^3}W^2\right) \times 2^{N_0+c_1} \\
k_2 = \dfrac{f_T}{c}\left(\dfrac{a}{f_c^2}W + \dfrac{\hat{a}}{f_c^3}W^2\right) \times 2^{N_0+c_1+c_2} \\
k_3 = \dfrac{f_T\hat{a}}{cf_c^3}W^2 \times 2^{N_0+c_1+c_2+c_3}
\end{cases}
\tag{6}
$$

As *Fig. 5* shows, even under different jerk rates, the hybrid-clock third-order DDS can maintain high Doppler simulation accuracy, and the Doppler frequency shift error is always less than 2 mHz. The table compares resource and power consumption results of the latter two accumulators for cases of W = 1 and W = 10, detailing the differences in static power consumption and dynamic power consumption for these two values of W.

To compare the simulation results to an actual unit, the FPGA used for analysis in the table was a model XC6SLX150 from Xilinx (www.xilinx.com), and the power consumption analysis was produced with the aid of an XPower Analyzer from Xilinx. For W = 10, the accumulation clock rate of the last two DDS accumulator stages is reduced to 1/W of the same-clock condition, which results in a dynamic power consumption reduction of approximately 1/W.

The XC6SLX150 FPGA is a member of the firm's Spartan-6 family of products, with each FPGA in the product line incorporating as many as six clock management tiles (CMTs), with each CMT consisting of two digital clock managers (DCMs) and one phase-locked loop (PLL), which can be used individually or cascaded. The model XC6SLX150 FPGA features 147,443 logic cells and more than 23,000 configurable logic slices. The integrated device makes use of more than 184,000 flip-flops and 1355 kb maximum distributed random access memory (RAM) to provide its performance with relatively low static power consumption and low dynamic power consumption. It was considered a good subject for investigation with the model, since it offers performance and capabilities that can be used across a wide range of DDS applications, and would represent a good "typical" FPGA for modeling purposes.

This hybrid-clock third-order DDS model developed here is fairly straightforward and can be used under both same-clock and hybrid-clock DDS conditions, and can be used to predict the amount of power consumption under static as well as dynamic conditions. The simulation results for the BeiDou2 B1 carrier signal show that the signal Doppler simulation method achieves precision of 2 mHz. Compared with the same-clock condition, the third-order DDS under hybrid-clock conditions operates with less resource requirements and power consumption. The model offers an effective method for projecting the amount of power that will be required by a given FPGA product when employed as part of a DDS system. This simulation approach provides a means of precisely simulating Doppler signals, and is particularly useful for modeling portable high-dynamic-range satellite navigation equipment. mw

Editor's Note: For an expanded version of this article, including a full listing of equations, visit www.mwrf.com/systems/dds-model-tunes-doppler-simulation.

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