Design Feature

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# PLL Synthesizer Provides Fast Locking

## A dual charge-pump structure combined with a dynamic loop-bandwidth technique serves to improve the phase-locking performance of a 1.4- to1.6-GHz frequency synthesizer.

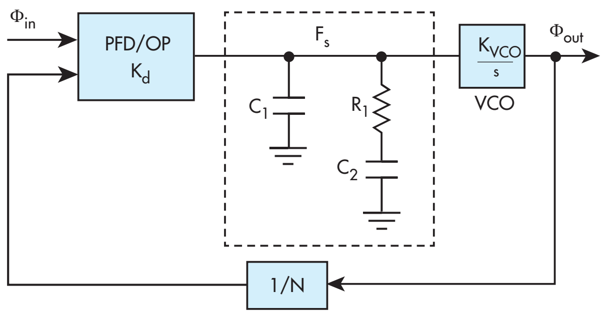
Frequency synthesizer lock time is a key parameter in many systems, especially for those in which frequency tuning speed is essential. Short lock times translate into fast tuning speeds and help make signals difficult to track—an important attribute in many military and business operations.

In pursuit of fast locking time, a simplified phase-locked-loop (PLL) frequency synthesizer was developed. It provides low phase noise and low spurious levels based on a dynamic loop-bandwidth technique which has a controllable charge-pump current and dual-charge-pump structure. Its lock time is just 4.8 μs. The phase noise ranges from –100 to –105 dBc/Hz within the loop bandwidth, with spurious suppression of better than –63 dBc for the frequency band of 1.4 to 1.6 GHz.

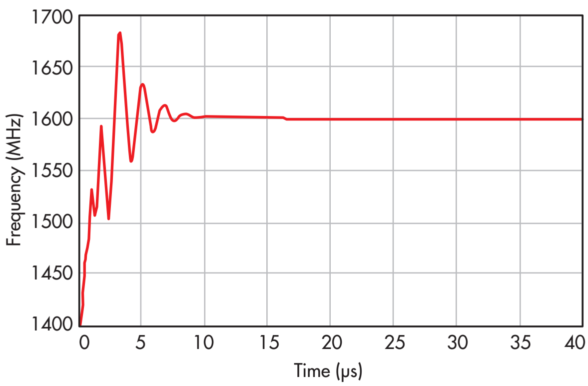
There are several ways to boost the locking speed of a PLL frequency synthesizer. The preset voltage technique can provide a preset tuning voltage for the synthesizer's voltage-controlled oscillator (VCO) to tune the oscillator's output frequency closer to the target frequency and reduce the total time needed for tuning to that target frequency. Because the speed of lookup functions and digital-to-analog-converter (DAC) circuits are in the range of nanoseconds—much faster than the typical locking time of PLLs, which is in the range of microseconds—the preset voltage technique is, in theory, the fastest method available.

However, the control module used with the PLL preset voltage technique is very complex, which can mean increased cost and larger circuit size. The dynamic loop bandwidth technique changes the loop bandwidth in different stages. It can boost the locking speed while achieving low phase noise and low spurious levels. Yet, switching the loop bandwidth can introduce frequency jitter, which may increase the locking time; the loop bandwidth is limited by the phase comparison frequency of this approach.

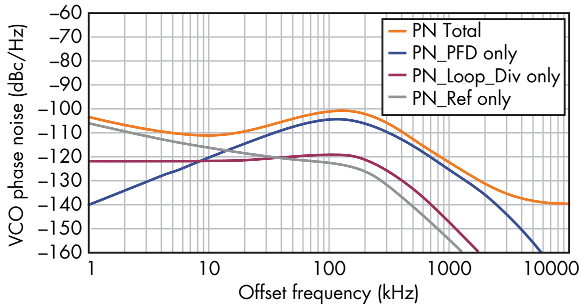
The fractional-N technique uses a higher phase comparison frequency which means a wide loop bandwidth and lower division ratio than for an integer-N frequency synthesizer.[1] This approach enables low-frequency phase noise to be suppressed to a high degree.[2,3] For optimum performance and fast locking times, the fractional-N and dynamic loop bandwidth techniques were combined. The sigma-delta technique can be applied to




**1. This block diagram represents a simplified PLL system with second-order loop filter.**




**2. The plot is a simulation of PLL synthesizer locking time with a model ADF4154 as the phase-frequency detector (PFD).**




**3. The plot is a simulation of PLL synthesizer phase noise with a model ADF4154 as the PFD.**

help suppress fractional spurious levels, meaning a wider loop bandwidth can be used under steady-state conditions to speed the locking time even more.[4,5]

To better understand the dynamic loop bandwidth method for speeding the tuning time of PLL frequency synthesizers, it is necessary to review the relationship between synthesizer loop bandwidth and PLL locking time. A nonlinear relationship describing the loop module is needed to accurately calculate the locking time. Based on a simplified PLL system *(Fig. 1)*, the transmission function of the loop's low-pass filter can be found from Eq. 1:

$$F(s) = \frac{1+sC_2R_2}{s(C_1+C_2)(1+s\frac{C_1C_2R_1}{C_1+C_2})} = \frac{1+sT}{sA_0(1+s\frac{A_1}{A_0})} \quad (1)$$

where

$A_0 = C_1 + C_2$;
$A_1 = C_1C_2R_1$; and
$T = R_1C_2$.

Because the high-order term has little impact, the system transmission function can be simplified to the relationship of Eq. 2:

$$H(s) \approx \frac{KTs+K}{A_0s^2+\frac{T_2K}{N}s+\frac{K}{N}} = \frac{2N\xi\omega_n s+N\omega_n^2}{s^2+2\xi\omega_n s+\omega_n^2} \quad (2)$$

with

$$(\omega_n = \sqrt{\frac{K}{A_0N}},\ \xi = \frac{T}{2}\omega_n)$$

The locking time for closing the loop[6] can be found from Eq. 3:

$$t_{lock} = \frac{2}{\omega_{BW}}\ln\frac{\Delta f}{(f_1+\Delta f)|\alpha|} \quad (3)$$

The loop bandwidth of the second-order filter is $\omega_{BW} = 2\zeta\omega_n$, so that Eq. 4 can be applied:

$$t_{lock} = \frac{1}{\zeta\omega_n}\ln(\frac{\Delta f}{(f_1+\Delta f)|\alpha|}) \quad (4)$$

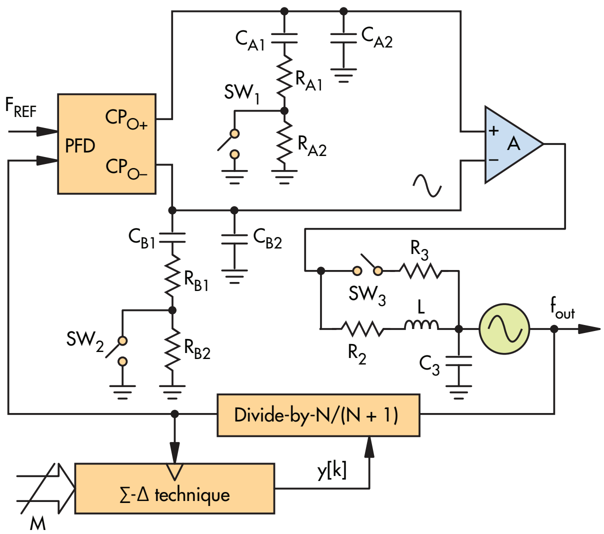
When the frequency jumps from 1.4 to 1.6 GHz, the locking time of the structure shown in *Fig. 1* with a 600-kHz loop bandwidth and frequency deviation of 10 ppb (10 Hz) can be calculated by means of Eq. 5:

$$t_{600kHz} = \frac{2}{2\pi\times600\times10^3}\ln\frac{(1.6-1.4)\times10^9}{1.6\times10^9\times|10\times10^{-9}|} = 8.67\mu s \quad (5)$$

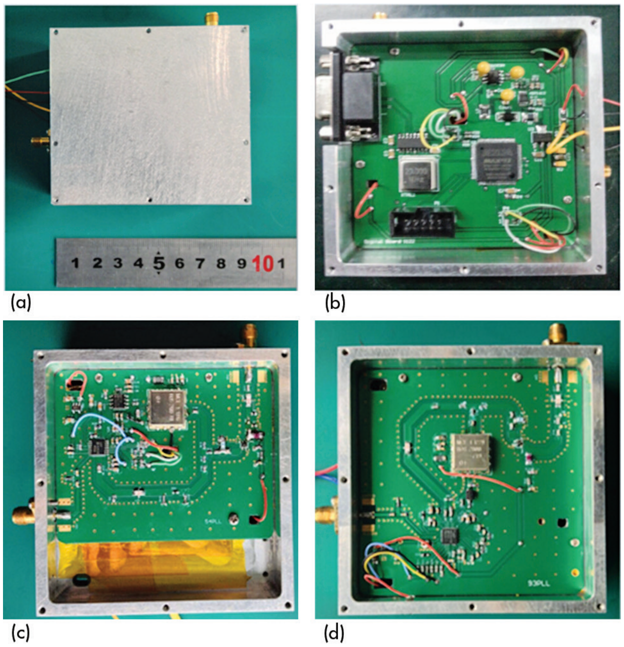
When the loop bandwidth changes to 150 kHz, the locking time can be found by means of Eq. 6:

$$t_{150kHz} = \frac{2}{2\pi\times150\times10^3}\ln\frac{(1.6-1.4)\times10^9}{1.6\times10^9\times|10\times10^{-9}|} = 34.7\mu s \quad (6)$$

As the loop bandwidth widens, shorter lock times can be obtained. The loop bandwidth is proportional to $\omega_n$, and $\omega_n$ is proportional to $(I_p)^{0.5}$, so it's possible to achieve a dynamic loop bandwidth by changing the charge pump current $I_p$. Analog Devices' (www.analog.com) ADF4154 phase-frequency detector (PFD) was chosen for the PLL due to its controllable charge pump current. Current is controllable in 12 grades with a minimum value of 313 µA and maximum value of 5 mA.




**4. This block diagram is an improved approach for increasing the locking time of a PLL frequency synthesizer.**




**5. The photographs illustrate different aspects of the two fabricated PLL frequency synthesizers: (a) overall dimensions, (b) the control module, (c) the frequency synthesizer with a model ADF4154 as the PFD, and (d) the frequency synthesizer with a model ADF4193 as the PFD.**

A value of 313 µA was selected as the standard to design the loop structure and control $I_p$ to be 5 mA in fast-locking mode, thus quadrupling the loop bandwidth and achieving fast-locking operation. The design was simulated using the Advanced Design System (ADS) simulation software from Agilent Technologies [now Keysight Technologies (www.keysight.com)], which indicates that the locking time is close to 14 µs *(Fig. 2)* and the phase noise is –102 dBc/Hz offset 1 kHz from the carrier *(Fig. 3)*.

To further improve fast-locking PLL performance, a difference loop structure was designed with a dual-charge-pump output to increase the locking progress *(Fig. 4)*. The PFD was changed from a model ADF4154 to a model ADF4193, also from Analog Devices. Model ADF4193 is a fractional-N PFD with differential dual-output configuration. The charge pump features 64 parallel charge-pump units, each of which can provide 100-µA current. In fast-locking model, the loop bandwidth of the PLL system increases eight-fold with the full workings of the entire 64 charge-pump units, shortening the PLL lock time.

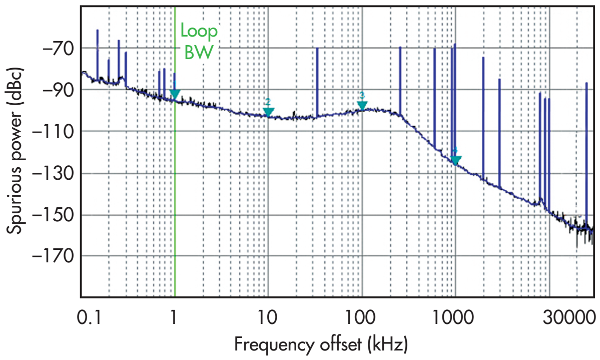
In the system shown in *Fig. 4*, when the phase error of the two input signals of a PFD increases positively, the charge pump provides the loop filter with a source current that is integrated by the loop filter structure to control the VCO. This source current makes the phase of VCO's output carrier signal approach the reference frequency phase. Conversely, when the phase error of the two input signals of the PFD increases negatively, the charge pump absorbs the sink current from the loop filter to make the phase of VCO's output signal close to the phase of the reference frequency via a negative adjustment. The final goal is for the phase error of the VCO's output and the reference frequency to become zero.

The model shown in *Fig. 4* describes the process for a PLL frequency synthesizer with a single charge pump. In a charge pump with two outputs (CP0+ and CP0–, when the phase error between two input signals to the PFD increases positively, the CP0+ delivers the source current to increase the voltage of the integral capacitance linked to the CP0+ port. At the same time, output CP0- absorbs the sink current to reduce the voltage of the integral capacitance linked to the CP0- port, quickly increasing the voltage difference between the CP0+ and CP0- outputs.

The difference charge pump largely improves the degree of mismatch between the source current and the sink current that will optimize the spurious performance. In doing so, it provides more freedom of design for the loop filter. Moreover, in the design shown in *Fig. 4*, when the loop bandwidth increases, switch $SW_3$ is triggered to reduce the charging resistance of the capacitance linked to the OPA's output port. This will lead to an increase in charge current. This reduces the time of reaching a certain tuning voltage even more.

However, the other parameters of the system changed with the loop width—especially the damping factor, which increases with the charge pump current and may also affect the time constant. To keep the damping factor unchanged, it is necessary to adjust R1 proportionally with the change of $I_p$ to stabilize the loop as

**6. The oscilloscope screenshots show the lock times for the PLL synthesizers, with (left) a 150-kHz static loop bandwidth, (middle) a model ADF4154 as the PFD, and (right) a model ADF4193 as the PFD.**




**7. This plot of phase noise was measured for an output frequency of 1531 MHz.**

shown in *Figure 4*. In this program, switches $SW_1$ and $SW_2$ are triggered to shorten RA2 and RB2 when the charge-pump current $I_p$ increases multiply to keep the damping factor unchanged. To demonstrate the effectiveness of combining these methods for enhanced PLL synthesizer tuning speed, two PLL frequency synthesizers were fabricated with commercial PFDs. One used a model ADF4154 as the PFD; the other used a model ADF4193 as the PFD *(Fig. 5)*. The lock times of the two were compared.

An indirect measurement approach was used to determine the synthesizer lock times. It considers the enable signal $L_E$ as the trigger pulse and then measures the tuning voltage.[7] *Figure 6* compares the lock times for the synthesizers with a 150-kHz static loop bandwidth, when using the model ADF4154 as the PFD, and the model ADF4193 as the PFD. For the static loop bandwidth of 150 kHz and a 200-MHz frequency step, the lock time is 30 µs. This is close to the value of 34.7 µs computed by Eq. 6. This illustrates that Eq. 3 has reference values.

Using the improved structure and the dynamic loop bandwidth technique employed with the ADF4154 as the PFD, the PLL synthesizer lock time is 13.8 µs. This is somewhat longer than the computed result of 8.67 µs from Eq. 5, achieving a loop bandwidth of 600 kHz. This indicates that the dynamic-loop-bandwidth technique helps speed synthesizer lock time. By combining the dynamic-loop-bandwidth technique and the difference dual-charge-pump structure, it is possible to produce a frequency synthesizer with lock time of just 4.8 µs.

*Figure 7* shows the spurious performance for an output frequency of 1531 MHz with a model ADF4193 as the PFD. When the frequency span is 1 MHz, spurious suppression is better than –63 dBc with phase-noise performance of –94.6 dBc/Hz offset 1 kHz from the carrier *(Fig. 8 and table)*. Within the loop bandwidth, the phase noise ranges from –100 to –105 dBc/Hz. The maximum spurious level of about –66 dBc occurs at a 1-MHz offset frequency. Fractional spurious signals occur at offsets of 2 and 3 MHz; the spurious suppression is better than –70 dBc.

**PLOTTING PHASE NOISE AT 1531 MHz**

| Marker | Offset frequency | Phase noise |
|---|---|---|
| 1 | 1 kHz | -94.57 dBc/Hz |
| 2 | 10 kHz | -103.22 dBc/Hz |
| 3 | 100 kHz | -100.13 dBc/Hz |
| 4 | 1 MHz | -126.43 dBc/Hz |

In short, Eq. 3 expresses the relationship between loop bandwidth and PLL synthesizer locking time. The dynamic-loop-bandwidth technique was applied to speed locking time; it allows a higher loop bandwidth during frequency tracking to achieve fast locking times. A frequency synthesizer was fabricated with the model ADF4154 PFD that achieved locking time of only 13.8 µs. To further shorten the locking time, a design structure was developed employing the difference between dual-charge-pump outputs to accelerate the speed of changing voltages. By fabricating a PLL frequency synthesizer with the model ADF4193 phase-frequency detector, a lock time of just 4.8 µs was achieved, which equates to an improvement of 9 µs. mw

ACKNOWLEDGMENT

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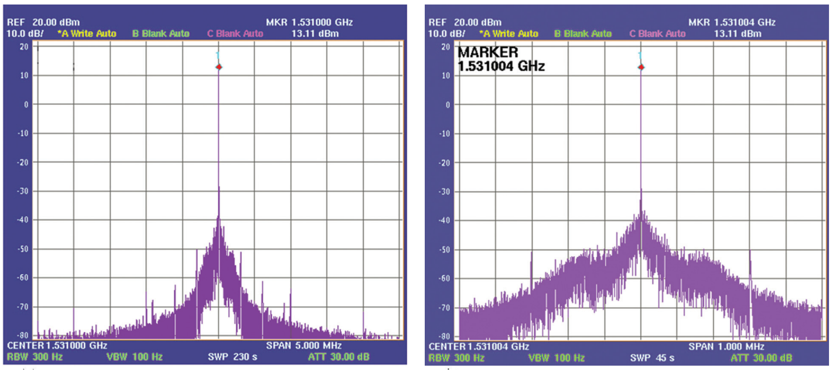


**8. These screenshots show two frequency spans for an output frequency of 1531 MHz: (left) a span of 5 MHz and (right) a span of 1 MHz.**